EC COURSE FILE

Contents required for course file

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1.	Cover page	
2.	Syllabus copy	
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4.	Mission of the department	
5.	PEO's and PO's	
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7.	Brief notes on the importance of the course and how it fits into the curriculum	
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10.	Course mapping with POs	
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21.	Known gaps, if any inclusion of the same in lecture schedule	
22.	Discussion topics, if any	
23.	References, Journals, websites and E-links if any	
24.	Quality Control Sheets a. Course end survey b. Teaching Evaluation	
25.	Students List	
26.	Group-Wise students list for discussion topics	

GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ***Electronics and communications Engineering***

(Name of the Subject / Lab Course) : Electronic circuits

(JNTU CODE -) A40413 **Programme :** ***UG***

Branch: EEE	**Version No :**
Year: II	**Updated on : 05/12/2015**
Semester: II	**No. of pages :**

Classification status (Unrestricted / Restricted)

Distribution List :

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4) Date : 20/12/2014	**4) Date :**

Verified by : 1) Name :	*** For Q.C Only.**
2) Sign :	**1) Name :**
3) Design :	**2) Sign :**
4) Date :	**3) Design :**
	4) Date :

Approved by : (HOD) 1) Name :

2) Sign :

3) Date :

2.Syllabus copy

JAWAHARLAL NEHRU TECHNOLOGIVAL UNIVERSITY HYDERABAD
II YEAR B.TECH EEE I-SEM

L	T/P/D	C
4	-/-/-	4

ELECTRONIC CIRCUITS

Objective:

Electronic Circuits plays significant role in day to day life of entire mankind. This course deals with the concept of different types of amplifiers, oscillators, vibrators, clippers, clampers, switching characteristics of various semi conductor devices, linear wave shaping and frequency response of bipolar junction transistor and field effect transistor.

UNIT I

Single Stage Amplifiers Design And Analysis: Review of CE,CB,CC & CS amplifiers-classification of amplifiers, Distortion in Amplifiers-Approximate analysis, CE,CB,CC amplifiers comparison.

FEEDBACK AMPLIFIERS: concepts of feedback, classification of feedback amplifiers, General characteristics of negative feedback amplifiers, Effect of feedback on amplifier characteristics-Voltage shunt voltage series, Current shunt and current series feedback configurations. Simple Problems.

UNIT -II BJT & FET Frequency Response: Logarithms, Decibels, General frequency considerations, Low Frequency analysis, Low Frequency response of BJT Amplifier- Low Frequency response of FET Amplifier, Miller effect capacitance-High Frequency response of BJT Amplifier- Square Wave testing

UNIT -III

MULTIVIBRATORS: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using transistors.

Clippers and Clampers : Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper, Comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Transfer characteristics of clampers.

UNIT -IV

Large signal amplifiers: class A Power amplifier, Maximum value of efficiency of class A amplifier, Transformer coupled amplifier,-push pull amplifier-complimentary symmetry circuits(transformer less class B Power amplifier)-Phase inverters, Transistor power dissipation, Thermal run away, heat sinks.

LINEAR WAVE SHAPING: High pass, low pass RC circuits, their response for sinusoidal, step, pulse, square and ramp inputs.

UNIT -V

SWITCHING CHARACTERISTICS OF DEVICES : Diode as a switch, piecewise linear diode characteristics, Transistor as a switch, Break down voltage consideration of transistor, saturation parameters of Transistor and their variation with temperature, Design of transistor switch, transistor-switching times.

TEXT BOOKS:

1. Electronic Devices and Circuit Theory, Robert L.Boylestad, Louis Nasheisky, 9th edition 2007,Pearson Education.
2. Electronic Devices and Circuits by S.Salivahanan, N.Suresh Kumar and A.Vallavaraj, 2nd Edition., 2008, TMH.
3. Solid State Pulse circuits by David A. Bell, PHI, 4th Edition.

REFERENCE BOOKS:

1.Introductory Electronic Devices and Circuits(conventional flow version)-Robert T.Paynter,7th edition,2009,PEI.

2. Electronic Devices and Circuits – Anil K. Maini, Varsha Agarwal, 1 Ed., 2009, Wiley

3. Pulse, Digital and Switching Waveforms - J. Millman, H. Taub and Mothiki S Prakash rao,2nd edition,TMH.

Outcomes:

After going through this course the students gets a thorough knowledge on various electronic circuits like oscillators, multivibrators, frequency response analysis, clippers and clampers,swithching characteristics of semi conductor devices, concept of wave shaping, with this knowledge they can apply sufficient knowledge for solving real world problems.

3. Vision Of The Department

To provide excellent Electrical and electronics education by building strong teaching and research environment

4. Mission of the Department

1. To offer high quality graduate program in Electrical and Electronics education and to prepare students for professional career or higher studies.
2. The department promotes excellence in teaching, research, collaborative activities and positive contributions to society

5. Programme Educational Objectives(EEE)

PEO 1. Graduates will excel in professional career and/or higher education by acquiring knowledge in Mathematics, Science, Engineering principles and Computational skills.

PEO 2. Graduates will analyze real life problems, design Electrical systems appropriate to the requirement that are technically sound, economically feasible and socially acceptable.

PEO 3.Graduates will exhibit professionalism, ethical attitude, communication skills, team work in their profession, adapt to current trends by engaging in lifelong learning and participate in Research & Development.

5.Programme Outcomes (EEE)

PO 1. An ability to apply the knowledge of Mathematics, Science and Engineering in Electrical and Electronics Engineering.

PO 2. An ability to design and conduct experiments pertaining to Electrical and Electronics Engineering.

PO 3. An ability to function in multidisciplinary teams

PO 4. An ability to simulate and determine the parameters such as nominal voltage current, power and associated attributes.

PO 5. An ability to identify, formulate and solve problems in the areas of Electrical and Electronics Engineering.

PO 6. An ability to use appropriate network theorems to solve electrical engineering problems.

PO 7. An ability to communicate effectively.

PO 8. An ability to visualize the impact of electrical engineering solutions in global, economic and societal context.

PO 9. Recognition of the need and an ability to engage in life-long learning.

PO 10 An ability to understand contemporary issues related to alternate energy sources.

PO 11 An ability to use the techniques, skills and modern engineering tools necessary for Electrical Engineering Practice.

PO 12 An ability to simulate and determine the parameters like voltage profile and current ratings of transmission lines in Power Systems.

PO 13 An ability to understand and determine the performance of electrical machines namely speed, torque, efficiency etc.

PO 14 An ability to apply electrical engineering and management principles to Power Projects.

6. Course objectives and Outcomes

Course objectives

Electronic Circuits plays significant role in day to day life of entire mankind. This course deals with the concept of different types of amplifiers, oscillators, vibrators, clippers, clampers, switching characteristics of various semi conductor devices, linear wave shaping and frequency response of bipolar junction transistor and field effect transistor.

Course outcomes

CO1: Describe classification of amplifiers and their analysis of CE, CB, CC amplifiers using hybrid model and derive for voltage, current gain, input impedance and output impedance.

CO2: Design and analyze single stage amplifiers and their frequency response, its gain band width product and effect of coupling and bypass capacitors in amplifiers.

CO3: Solve and design the characteristics of the different types of feedback amplifiers.

CO4: Describe the condition for oscillations in oscillators and design different types of oscillators and analyze their frequency of operations.

CO5: Design and analyze different types of power amplifiers and compare them in terms efficiency.

CO6 : Able to design non-linear wave shaping circuits Clippers and Clampers.

CO7: Able to Use diodes and transistors as switches.

CO8: Able to Analyze and design multivibrators .

After going through this course the students gets a thorough knowledge on various electronic circuits like oscillators, multivibrators, frequency response analysis, clippers and clampers,swithching characteristics of semi conductor devices, concept of wave shaping, with this knowledge they can apply sufficient knowledge for solving real world problems.

7. Brief notes on the importance of the course and how it fits into the curriculum

Electrical engineers need to understand the intimate relationship between frequency and time. Circuits can

be characterized both in time and frequency domain. It is important that an electrical engineer be able to travel between these two worlds effortlessly. Sometimes, a circuit problem that is difficult in one domain can be easily analyzed in the other domain. A good place to begin the study of the time-frequency relationship is in the design and analysis of a transistor amplifier circuit.

Electronic Circuits describe the students to electronics circuits that they are used in modern devices and electronic systems. The course will start with discussion of configuration of BJT, frequency response of amplifiers. electronic circuits including amplifiers, diode circuits (small signal model, rectifiers, clamping circuits, etc), the FET transistor analysis and its equivalent circuits, biasing, DC analysis of amplifier circuits, single stage amplifiers .

The study of EEE can involve large amounts of power (eg power and control engineering) and large devices (eg power stations and electric vehicles) or small amounts of power (eg computer, communications and information engineering) and small devices (eg MP3 players and cell phones)

8. Prerequisites if any

- Electronic Devices and circuits: PN Junction Diode, BJT,FET
- Physics: p type and n-type materials
- mathematics : Different ion, integration

9.Instructional Learning Outcomes

Learning outcomes are the key abilities and knowledge that will be assessed

1.Single Stage Amplifiers Design and analysis,FeedbackAmplifiers

Students are able to

1. Know the classification of amplifiers and distortion of amplifiers.
2. Describe the analysis of CE amplifier using hybrid model and derive for voltage, current gain, input impedance and output impedance.
3. Describe the analysis of CB amplifier using hybrid model.
4. Describe the analysis of CC amplifier using hybrid model.
5. Know the millers theorem and its applications in analysis amplifiers.
6. Design of single stage RC coupled amplifier using BJT.
7. Know the basic concept of feedback and its effect on the operation of an amplifier.
8. Describe the different types of the feedback amplifiers.
9. Describe the general characteristics of negative feedback amplifiers.
10. Solve and design characteristics of the voltage series and voltage shunt feedback amplifiers.
11. Solve and design the characteristics of the current series and current shunt feedback amplifiers.

2.BJT & FET Frequency Response

Students are able to

1. Know the logarithms, decibels, frequency considerations of an amplifier.
2. Analyze the frequency response of an amplifier at low and high frequencies.
3. Describe and analyze the effect of coupling and bypass capacitors in amplifiers.
4. Design and analyze single stage CE amplifier frequency response and its gain band width product.
5. Design and analyze single stage Emitter follower amplifier frequency response at higher frequency.

3.Multivibrators , Clippers and Clamppers

Students are able to

1. Explain the principle of operation of the multivibrators.
2. Analyze and design Bistable, Monostable and Astable multivibrators and able to calculate and frequency / pulse width of the generated signal.
3. Plot the waveforms at various points in the circuit.
4. Describe the emitter coupled astable multivibrators
5. Use an astable multivibrator for applications such as voltage to frequency converter and frequency modulator
6. Understand the working of emitter coupled monostable multivibrator
7. Realize the need for a commutating condenser in a monostable multivibrator and bistable multivibrator.
8. Realize the application of a monostable multivibrator as a voltage to time converter
9. Analyze fixed bias and self bias bistable multivibrators
10. Analyze and design emitter coupled bistable multivibrator, also called Schmitt trigger
11. Describe the applications of bistable multivibrator circuits.

Students are able to

1. Design various series and shunt clipping circuits and their combinations.
2. Understand the principle of operation of two level emitter coupled transistor clippers and noise clippers
3. Describe simple diode comparators and double differentiators as amplitude comparators.
4. Explain the applications of comparators.
5. Design various clamping circuits and verify the clamping circuit theorem.
6. Derive the necessary relations to plot steady state output.
7. Describe the effect of diode characteristics on the clamping voltage.
8. Describe synchronized clamping.
9. State and derive the clamping circuit theorem

4.Large signal amplifiers ,Linear Wave Shaping

Students are able to

1. Describe the classification of large signal amplifiers.
2. Design and analyze transformer coupled class A audio power amplifier.
3. Design and analyze class B amplifier and its efficiency.
4. Design and analyze class B push pull and complementary amplifiers.
5. Compare class A, B, AB amplifiers.
6. Know about thermal stability and heat sinks.

5.Switching Characteristics of Devices

Students are able to

1. Use diodes and transistors as switches.
2. Describe the effect of inter-electrode capacitances on switching times.
3. Describe the switching times of devices and derive the necessary relations.
4. Describe the temperature dependence of the transistor on various parameters.
5. Understand the use of transistor switch as latch.

10. Course mapping with PEOs and Pos

	PROGRAMME EDUCATIONAL OBJECTIVES					
	Domain knowledge	**Professional Employment**	**Higher Degrees**	**Engineering citizenship**	**Lifelong Learning**	**Research and Development**
a) an ability to apply the knowledge of Mathematics, science and engineering in Electronics and communications	√	√	√		√	√
b) an ability to Design & Conduct Experiments, as well as analyze & Interpret Data	√	√	√		√	√
c) an ability to design a system, component, or process to meet desired needs with in realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability	√	√	√		√	√
e) an ability to Identify, Formulate & Solve problems in the area of Electronics and Communications Engineering	√	√	√		√	√

i) a recognition of the need for, and an ability to engage in life-long learning	√	√	√		√	√
k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice	√	√	√		√	√

Relationship of the course to the program educational objectives :

1. **Domain knowledge:** Graduates will be able to synthesize mathematics, science, engineering fundamentals, laboratory and work-based experiences to formulate and solve engineering problems in Electronics and Communication engineering domains and shall have proficiency in Computer-based engineering and the use of computational tools.	√
2. **Professional Employment:** Graduates will succeed in entry-level engineering positions within the core Electronics and Communication Engineering, computational or manufacturing firms in regional, national, or international industries and with government agencies.	√
3. **Higher Degrees:** Graduates will succeed in the pursuit of advanced degrees in Engineering or other fields where a solid foundation in mathematics, science, and engineering fundamentals is required.	√
4. **Engineering citizenship:** Graduates will be prepared to communicate and work effectively on team based engineering projects and will practice the ethics of their profession consistent with a sense of social responsibility.	
5. **Lifelong Learning:** Graduates will recognize the importance of, and have the skills for, continued independent learning to become experts in their chosen fields and to broaden their professional knowledge.	√
6. **Research and Development:** To undertake Research and Development works in the areas of Electronics and Communication fields.	√

11.Time table of concerned class

12. Individual time table

Faculty Name: B.MAMATHA (22)				SUB: EDC (CSE 3C, IT 2A)		EE LAB: CSE 2A & 2C, IT 2A, MECH 2A (A1)		
Time	**09.30-10.20**	**10.20-11.10**	**11.10-12.00**	**12.00-12.50**	**12.50-13.30**	**13.30-14.20**	**14.20-15.10**	**15.10-16.00**
Period	**1**	**2**	**3**	**4**		**5**	**6**	**7**
Mon		**EC&PC LAB(2-2B1)**			**LUNCH**			
Tue	**ESD**	**ESD**				**EC**		
Wed	**EC**	**EC&PC LAB(2-2B1)**						
Thur		**EC**						
Fri				**EC**				
Sat						**EC**		

13 .Lecture schedule with methodology being used/adopted

Geethanjali College of Engineering & Technology

Cheeryal(V), Keesara(M), R.R(D)

Department of **Electronics & Communications Engineering**

Year & Semesters to whom subject is offered **II-II EEE(A)**

Name of the Subject **Electronic Circuits**

Name of the Faculty: **B.Mamatha** Designation: **Assistant Professor** Department: **ECE**

13.1 Introduction to the Subject

Modern trends in electronics, Communication and Entertainment applications, measurement and instrument applications, Defence applications and applications in medicine, Passive component, Active components, SI units.

13.2 Unit-Wise Objectives of the Subject

- analyze and design single stage amplifiers.
- analyze Feedback amplifiers.
- analyze BJT Low and High Frequency response.
- Understand different clippers and clampers
- analyze multivibrators.
- analyze Power amplifiers.
- understand, design & demonstrate, generation & processing of pulse wave, wave shaping & switching functions with non-linear elements.
- analyze the switching characteristics of transistor and diode

13.3 Subject outcomes

On successful completion of this subject, students will be able to:

After going through this course the students gets a thorough knowledge on various electronic circuits like oscillators, multivibrators, frequency response analysis, clippers and clampers,swithching characteristics of semi conductor devices, concept of wave shaping, with this knowledge they can apply sufficient knowledge for solving real world problems.

13.4 JNTU Syllabus with additional topics

S.No.	Unit No.	Topic	Additional Topics
1	**I**	**Single Stage Amplifiers Design And Analysis**	
2		Review of CE & CB amplifiers	
3		Review of CC & CS amplifiers	
4		classification of amplifiers	
5		Distortion in Amplifiers	
6		Approximate analysis, CE,CB amplifier	
7		Approximate analysis, CC amplifier comparison.	
8		**FEEDBACK AMPLIFIERS:** concepts of feedback	
9		classification of feedback and feedback amplifiers	
10		General characteristics of negative feedback amplifiers	
11		Effect of feedback on amplifier characteristics	
12		Voltage shunt voltage series feedback configurations	
13		Current shunt and current series feedback configurations	
14		Simple Problems.	
15		assignment	
16	**II**	**BJT & FET Frequency Response:** Logarithms, Decibels	
17		General frequency considerations	
18		Low Frequency analysis	
19		Low Frequency response of BJT Amplifier	
20		Low Frequency response of FET Amplifier	
21		Miller effect capacitance	
22		High Frequency response of BJT Amplifier	
23		Square Wave testing	
24		Simple problems and assignment	
25	**III**	**MULTIVIBRATORS:**	
26		Analysis and Design of Bistable Multivibrator	
27		Analysis and Design of mono stable Multivibrator	
28		Analysis and Design of astable Multivibrator	
29		Schmitt trigger using transistors	
30		**Clippers and Clampers :** Diode clippers	
31		Transistor clippers	
32		clipping at two independent levels	
33		Transfer characteristics of clippers	
34		Emitter coupled clipper	
35		Comparators	

36		applications of voltage comparators	
37		clamping operation, clamping circuits using diode with different inputs	
38		Clamping circuit theorem, practical clamping circuits	
39		effect of diode characteristics on clamping voltage	
40		Transfer characteristics of clampers.	
41		Problems and assignment	
42	**IV**	**Large signal amplifiers:** class A Power amplifier	
43		Maximum value of efficiency of class A amplifier	
44		Transformer coupled amplif	
45		push pull amplifier	
46		complimentary symmetry circuits(transformer less class B Power amplifier)	
47		Phase inverters	
48		Transistor power dissipation	
49		Thermal run away, heat sinks.	
50		**LINEAR WAVE SHAPING:** High pass RC circuits	
51		low pass RC circuits	
52		High pass RC circuit response for sinusoidal, step inputs	
53		High pass RC circuits response for square and ramp inputs	
54		Low pass RC circuit response for sinusoidal, step inputs	
55		High pass RC circuits response for square and ramp inputs	
56		Simple problems and assignment	
57	**V**	**SWITCHINGCHARACTERISTICS OF DEVICES :** Diode as a switch	
58		piecewise linear diode characteristics	
59		Transistor as a switch	
60		Break down voltage consideration of transistor	
61		saturation parameters of Transistor	
62		their variation with temperature	
63		Design of transistor switch transistor-switching times	
64		Simple problems and assignment	

13.5 Source of Information

13.5.1 TEXT BOOKS:

1. Electronic Devices and Circuit Theory, Robert L.Boylestad, Louis Nasheisky, 9th edition 2007,Pearson Education.
2. Electronic Devices and Circuits by S.Salivahanan, N.Suresh Kumar and A.Vallavaraj, 2nd Edition., 2008, TMH.

3. Solid State Pulse circuits by David A. Bell, PHI, 4th Edition.

13.5.2 REFERENCE BOOKS:

1.Introductory Electronic Devices and Circuits(conventional flow version)-Robert T.Paynter,7th edition,2009,PEI.

2. Electronic Devices and Circuits – Anil K. Maini, Varsha Agarwal, 1 Ed., 2009, Wiley

3. Pulse, Digital and Switching Waveforms - J. Millman, H. Taub and Mothiki S Prakash rao,2nd edition,TMH.

13.5.3 WEBSITES

1. www.basicelectronic.blogspot.com
2. www.modernelectronics.org
3. www.electronicsforyou.con
4. **www.npteliitm.ac.in**

13.5.4 JOURNALS

1. A Very Low Level DC Current Amplifier Using Photocoupler Negative Feedback Circuit .

2. On the class IF power amplifier design

3. A Ringing Surge Clamper Type Active Auxiliary Edge-Resonant DC Link Snubber-Assisted Three-Phase

13.6 Unit wise Summary

S.No	Uni	Total	Topics to be covered	Reg /	Teaching	Remark

.	t No.	no. of Periods		Additional	aids used LCD/OHP/BB	s
1	**I**	**15**	**Single Stage Amplifiers Design And Analysis**	Regular	BB	
2			Review of CE & CB amplifiers	Regular	BB	
3			Review of CC & CS amplifiers	Regular	BB	
4			classification of amplifiers			
5			Distortion in Amplifiers			
6			Approximate analysis, CE,CB amplifier	Regular	BB	
7			Approximate analysis, CC amplifier comparison.	Regular	OHP,BB	
8			**FEEDBACK AMPLIFIERS:** concepts of feedback	Regular	**OHP,BB**	
9			classification of feedback and feedback amplifiers	Regular	OHP,BB	
10			General characteristics of negative feedback amplifiers	Regular	OHP,BB	
11			Effect of feedback on amplifier characteristics	Regular	OHP,BB	
12			Voltage shunt voltage series feedback configurations	Regular	BB	
13			Current shunt and current series feedback configurations	Regular	BB	
14			Simple Problems.	Regular	BB	
15			assignment	Regular	BB	
16	**II**	**10**	**BJT & FET Frequency Response:** Logarithms, Decibels	Regular	OHP,BB	
17			General frequency considerations	Regular	OHP,BB	
18			Low Frequency analysis	Regular	OHP,BB	
19			Low Frequency response of BJT Amplifier			
20			Low Frequency response of FET Amplifier	Regular	OHP,BB	
21			Miller effect capacitance	Regular	OHP,BB	
22			High Frequency response of BJT Amplifier	Regular	BB	

23			Square Wave testing	Regular	BB	
24			Simple problems and assignment	Regular	BB	
25	**III**	**16**	**MULTIVIBRATORS:**	Regular	BB	
26			Analysis and Design of Bistable Multivibrator	Regular	BB	
27			Analysis and Design of mono stable Multivibrator	Regular	BB	
28			Analysis and Design of astable Multivibrator	Regular	BB	
29			Schmitt trigger using transistors	Regular	OHP,BB	
30			**Clippers and Clampers :** Diode clippers	Regular	OHP,BB	
31			Transistor clippers	Regular	BB	
32			clipping at two independent levels	Regular	OHP,BB	
33			Transfer characteristics of clippers	Regular	OHP,BB	
34			Emitter coupled clipper			
35			Comparators	Regular	OHP,BB	
36			applications of voltage comparators	Regular	BB	
37			clamping operation, clamping circuits using diode with different inputs	Regular	BB	
38			Clamping circuit theorem, practical clamping circuits	Regular	BB	
39			effect of diode characteristics on clamping voltage	Regular	OHP,BB	
40			Transfer characteristics of clampers.	Regular	OHP,BB	
41			Problems and assignment	Regular	OHP,BB	
42	**IV**	**15**	**Large signal amplifiers:** class A Power amplifier			
43			Maximum value of efficiency of class A amplifier	Regular	OHP,BB	
44			Transformer coupled amplif	Regular	OHP,BB	

45			push pull amplifier	Regular	BB	
46			complimentary symmetry circuits(transformer less class B Power amplifier)	Regular	OHP,BB	
47			Phase inverters	Regular	BB	
48			Transistor power dissipation	Regular	BB	
49			Thermal run away, heat sinks.	Regular	BB	
50			**LINEAR WAVE SHAPING:** High pass RC circuits	Regular	BB	
51			low pass RC circuits	Regular	OHP,BB	
52			High pass RC circuit response for sinusoidal, step inputs	Regular	OHP,BB	
53			High pass RC circuits response for square and ramp inputs	Regular	OHP,BB	
54			Low pass RC circuit response for sinusoidal, step inputs			
55			High pass RC circuits response for square and ramp inputs	Regular	OHP,BB	
56			Simple problems and assignment	Regular	OHP,BB	
57	**V**	**10**	**SWITCHINGCHARACTERISTICS OF DEVICES :** Diode as a switch	Regular	OHP,BB	
58			piecewise linear diode characteristics	Regular	OHP,BB	
59			Transistor as a switch	Regular	OHP,BB	
60			Break down voltage consideration of transistor	Regular	OHP,BB	
61			saturation parameters of Transistor	Regular	OHP,BB	
62			their variation with temperature	Regular	OHP,BB	
63			Design of transistor switch transistor-switching times	Regular	OHP,BB	
64			Simple problems and assignment			
65			Mid-II			

13.7 MICRO PLAN

S.No.	Unit No.	Total no. of Periods	Date	Topics to be covered	Reg / Additional	Teaching aids used LCD/OHP/BB	Remarks
1	**I**			**Single Stage Amplifiers Design And Analysis**			
1			**30/12/2014**	Review of CE & CB amplifiers	Regular		
2			**31/12/2014**	Review of CC & CS amplifiers	Regular		
3			**02/01/2015**	classification of amplifiers	Regular	BB	
4			**03/01/2015**	Distortion in Amplifiers	Regular	BB	
5			**06/01/2015**	Approximate analysis, CE,CB amplifier	Regular	BB	
6			**07/01/2015**	Approximate analysis, CC amplifier comparison. **Miller's Theorem**	**Additional**		
7			**08/01/2015**	**FEEDBACK AMPLIFIERS:** concepts of feedback **Positive Feedback**	**Additional**	BB	
8			**09/01/2015**	classification of feedback and feedback amplifiers			
9			**10/01/2015**	General characteristics of negative feedback amplifiers	Regular	OHP,BB	
10			**13/01/2015**	Effect of feedback on amplifier characteristics	Regular	BB	
11			**14/01/2015**	Voltage shunt voltage series feedback configurations			
12			**20/01/2015**	Current shunt and current series feedback configurations	Regular	OHP,BB	
13			**21/01/2015**	Simple Problems.	Regular	OHP,BB	
14			**23/01/2015**	assignment	Regular	OHP,BB	
15	**II**	**10**	**24/01/2015**	**BJT & FET Frequency Response:** Logarithms, Decibels	Regular	OHP,BB	
16			**27/01/2015**	General frequency considerations			
17			**28/01/2015**	Low Frequency analysis	Regular	OHP,BB	

18			**29/01/2015**	Low Frequency response of BJT Amplifier	Regular	OHP,BB	
19			**30/01/2015**	Low Frequency response of FET Amplifier	Regular	BB	
			31/01/2015	Miller effect capacitance	Regular	BB	
20			**03/02/2015**	High Frequency response of BJT Amplifier	Regular	BB	
21			**04/02/2015**	Square Wave testing **MOSFET Frequency Response**	**Additional**		
22			**05/02/2015**	Simple problems and assignment	Regular	BB	
23	**III**	**16**	**06/02/2015**	**MULTIVIBRATORS:**	Regular	BB	
24			**10/02/2015**	Analysis and Design of Bistable Multivibrator			
25			**11/02/2015**	Analysis and Design of mono stable Multivibrator	Regular	BB	
26			**12/02/2015**	Analysis and Design of astable Multivibrator	Regular	OHP,BB	
27			**13/02/2015**	Schmitt trigger using transistors	Regular	OHP,BB	
28			**18/02/2015**	**Clippers and Clampers :** Diode clippers	Regular		
29			**19/20/2015**	Transistor clippers	Regular	OHP,BB	
30			**20/02/2015**	clipping at two independent levels	Regular	OHP,BB	
31			**21/02/2015**	Transfer characteristics of clippers	Regular	OHP,BB	
32			**26/02/2015**	Emitter coupled clipper			
33			**27/02/2015**	Comparators	Regular	OHP,BB	
34			**28/02/2015**	applications of voltage comparators	Regular	OHP,BB	
35			**03/03/2015**	clamping operation, clamping circuits using diode with different inputs	Regular	BB	
36			**04/03/2015**	Clamping circuit theorem, practical clamping circuits			

37			**05/03/2015**	effect of diode characteristics on clamping voltage	**Additional**	BB	
38			**06/03/2015**	Transfer characteristics of clampers.	Regular	BB	
39			**07/03/2015**	Problems and assignment	Regular	BB	
40	**IV**	**15**	**10/03/2015**	**Large signal amplifiers:** class A Power amplifier			
41			**11/03/2015**	Maximum value of efficiency of class A amplifier			
42			**12/03/2015**	Transformer coupled amplif	Regular	BB	
43			**13/03/2015**	push pull amplifier	Regular	OHP,BB	
44			**14/03/2015**	complimentary symmetry circuits(transformer less class B Power amplifier)	Regular	BB	
45			**17/03/2015**	Phase inverters			
46			**18/03/2015**	Transistor power dissipation	Regular	OHP,BB	
47			**19/03/2015**	Thermal run away, heat sinks.	Regular	OHP,BB	
48			**20/03/2015**	**LINEAR WAVE SHAPING:** High pass RC circuits	Regular	OHP,BB	
49			**24/03/2015**	low pass RC circuits	Regular	BB	
50			**25/03/2015**	High pass RC circuit response for sinusoidal, step inputs	Regular	OHP,BB	
51			**26/03/2015**	High pass RC circuits response for	Regular	OHP,BB	
52			**27/03/2015**	Low pass RC circuit response for sinusoidal, step inputs	Regular	OHP,BB	
53			**28/03/2015**	High pass RC circuits response for square and ramp inputs	Regular	OHP,BB	
54			**31/03/2015**	Simple problems and assignment **Difference Between Linear and Non Linear Wave Shaping**	Regular **Additional**	OHP,BB	
55	**V**	**10**	**01/04/2015**	**SWITCHINGCHARACTE RISTICS OF DEVICES :** Diode as a switch	Regular	BB	
56			**02/04/2015**	piecewise linear diode characteristics	Regular	BB	

57			**03/04/2015**	Transistor as a switch	Regular	BB	
58			**04/04/2015**	Break down voltage consideration of transistor	Regular	OHP,BB	
59			**07/04/2015**	saturation parameters of Transistor	Regular	OHP,BB	
60			**08/04/2015**	their variation with temperature	Regular	OHP,BB	
61			**09/04/2015**	Design of transistor switch transistor-switching times	Regular	OHP,BB	
62			**10/04/2015**	Simple problems and assignment **Diode as A switch**	Regular **Additional**	OHP,BB	
63			**11/04/2015**	REVISION	Regular	OHP,BB	

13.8. Subject Contents

13.8. 1. Synopsis page for each period(62 pages)
13.8.2. Detailed Lecture notes containing:

1.ppts
2.ohp slides
3.subjective type questions(approximately 5 t0 8 in no)
4.objective type questions(approximately 20 to 30 in no)
5.Any simulations

13.9. Course Review (By the concerned Faculty):

(I)Aims

(II) Sample check

(III) End of the course rreport by the concerned faculty

GUIDELINES:

Distribution of periods :

No. of classes required to cover JNTU syllalbus : 50

No. of classes required to cover Additional topics : 5

No. of classes required to cover Assignment tests (for every 1 units 1 test) : 5

No. of classes required to cover tutorials : 5

No. of classes required to cover Mid tests : 2

No of classes required to solve University : 5

Question papers -------

Total periods 70

Total periods 70

14 .Detailed notes

UNIT-1

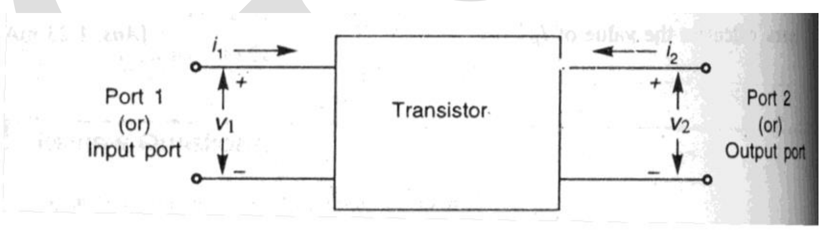
H – Parameter model :-

→ The equivalent circuit of a transistor can be dram using simple approximation by retaining its essential features.

→ These equivalent circuits will aid in analyzing transistor circuits easily and rapidly.

Two port devices & Network Parameters:-

→ A transistor can be treated as a two part network. The terminal behaviour of any two part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2, entering parts 1 & 2, respectively, as shown in figure.



Two port network

→ Of these four variables V_1, V_2, i_1 and i_2, two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two part parameters out of which the following three are more important.

1. Z – Parameters (or) Impedance parameters
2. Y – Parameters (or) Admittance parameters
3. H – Parameters (or) Hybrid parameters.

Hybrid parameters (or) h – parameters:-

→ If the input current i_1 and output Voltage V_2 are takes as independent variables, the input voltage V_1 and output current i_2 can be written as

$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$

$$i_2 = h_{21}\, i_1 + h_{22}\, V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11} = [V_1 / i_1]$ with $V_2 = 0$

= Input Impedance with output part short circuited.

$h_{22} = [i_2 / V_2]$ with $i_1 = 0$

= Output admittance with input part open circuited.

$h_{12} = [V_1 / V_2]$ with $i_1 = 0$

= reverse voltage transfer ratio with input part open circuited.

$h_{21} = [i_2 / i_1]$ with $V_2 = 0$

= Forward current gain with output part short circuited.

The dimensions of h – parameters are as follows:

h_{11} - Ω

h_{22} – mhos

h12, h21 – dimension less.

→ as the dimensions are not alike, (ie) they are hybrid in nature, and these parameters are called as hybrid parameters.

I = 11 = input ; 0 = 22 = output ;

F = 21 = forward transfer ; r = 12 = Reverse transfer.

Notations used in transistor circuits:-

$h_{ie} = h_{11e}$ = Short circuit input impedance

$h_{0e} = h_{22e}$ = Open circuit output admittance

$h_{re} = h_{12e}$ = Open circuit reverse voltage transfer ratio

$h_{fe} = h_{21e}$ = Short circuit forward current Gain.

The Hybrid Model for Two-port Network:-

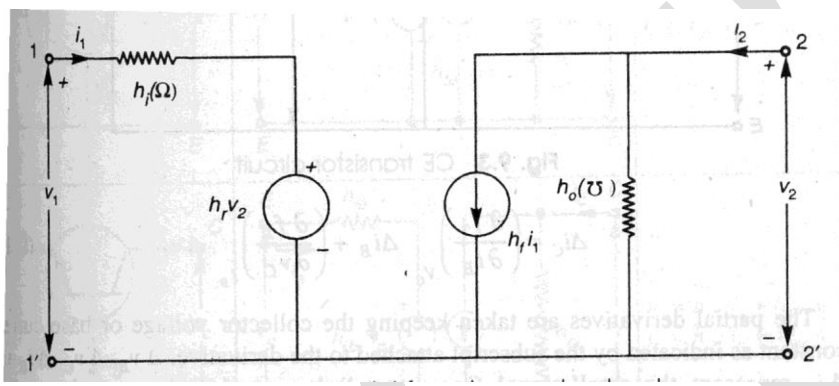
$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$

$$I_2 = h_1\, i_1 + h_{22}\, V_2$$

$$\downarrow$$

$$V_1 = h_1\, i_1 + h_r\, V_2$$

$$I_2 = h_f\, i_1 + h_0\, V_2$$



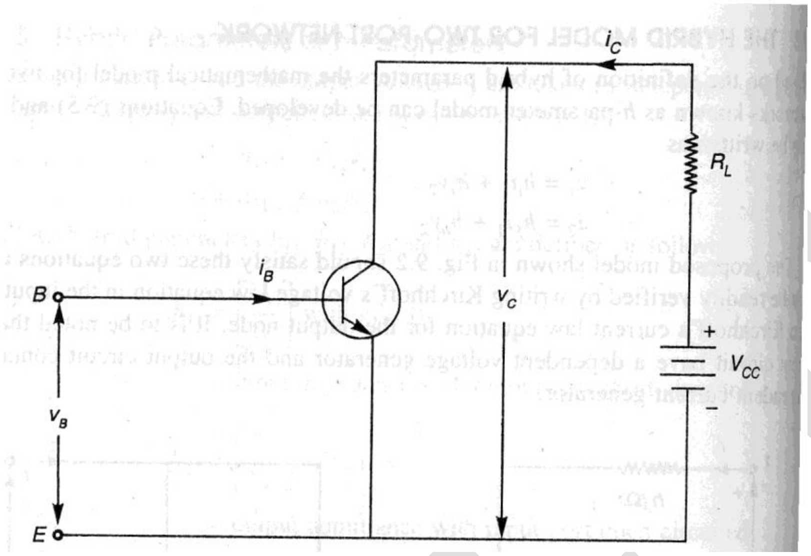
The Hybrid Model for Two-port Network

Transistor Hybrid model:-

Use of h – parameters to describe a transistor have the following advantages.

1. h – parameters are real numbers up to radio frequencies .
2. They are easy to measure
3. They can be determined from the transistor static characteristics curves.
4. They are convenient to use in circuit analysis and design.

5. Easily convert able from one configuration to other.
6. Readily supplied by manufactories.



CE Transistor Circuit

To Derive the Hybrid model for transistor consider the CE circuit shown in figure.The variables are i_{B}, i_c, $v_{B(=V_{BE})}$ and $v_{c(=V_{CE})}$. i_B and v_c are considered as independent variables.

Then , $v_B = f_1(i_B, v_c)$ ----------------------(1)

$i_C = f_2(i_B, v_c)$ ----------------------(2)

Making a Taylor's series expansion around the quiescent point I_B, V_C and neglecting higher order terms, the following two equations are obtained.

$$\Delta v_B = \left(\partial f_1/\partial i_B\right)_{V_C} . \Delta i_B + \left(\partial f_1/\partial v_c\right)_{I_B} . \Delta v_C \text{ ---------------(3)}$$

$$\Delta i_C = \left(\partial f_2/\partial i_B\right)_{V_C} . \Delta i_B + \left(\partial f_2/\partial v_c\right)_{I_B} . \Delta v_C \text{ ----------------(4)}$$

The partial derivatives are taken keeping the collector voltage or base current constant as indicated by the subscript attached to the derivative.

Δv_B , Δv_C , Δi_C , Δi_B represent the small signal(increment) base and collector voltages and currents,they are represented by symbols v_b , v_c , i_b and i_c respectively.

Eqs (3) and (4) may be written as

$$V_b = h_{ie}\, i_b + h_{re}\, V_c$$

$$i_c = h_{fe}\, i_b + h_{oe}\, V_c$$

Where $h_{ie} = \left(\partial f_1/\partial i_B\right)_{Vc} = \left(\partial v_B/\partial i_B\right)_{Vc} = \left(\Delta v_B /\Delta i_B\right)_{Vc} = \left(v_b / i_b\right)_{Vc}$

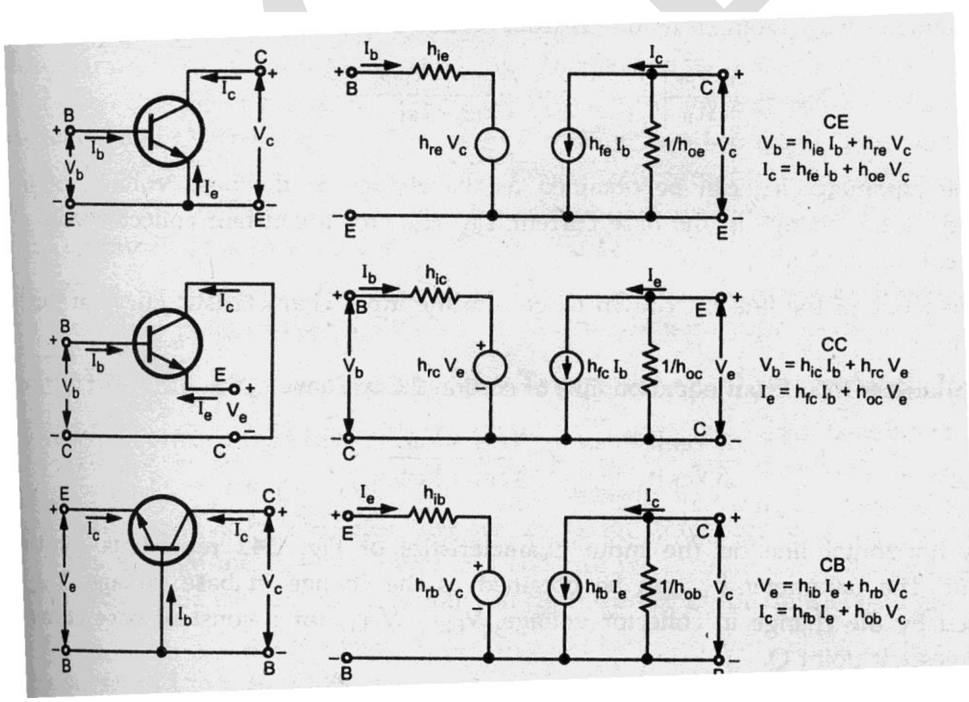
$h_{re} = \left(\partial f_1/\partial v_c\right)_{IB} = \left(\partial v_B/\partial v_c\right)_{IB} = \left(\Delta v_B /\Delta v_c\right)_{IB} = \left(v_b /v_c\right)_{IB}$

$h_{fe} = \left(\partial f_2/\partial i_B\right)_{Vc} = \left(\partial i_c /\partial i_B\right)_{Vc} = \left(\Delta i_c /\Delta i_B\right)_{Vc} = \left(i_c / i_b\right)_{Vc}$

$h_{oe} = \left(\partial f_2/\partial v_c\right)_{IB} = \left(\partial i_c /\partial v_c\right)_{IB} = \left(\Delta i_c /\Delta v_c\right)_{IB} = \left(i_c /v_c\right)_{IB}$

The above equations define the h-parameters of the transistor in CE configuration.The same theory can be extended to transistors in other configurations.

Hybrid Model and Equations for the transistor in three different configurations are are given below.



Simplified common emitter hybrid model:

UNIT-2

Frequency Response of Basic BJT and MOSFET Amplifiers

In this chapter you will learn about the general form of the frequency domain transfer function of an amplifier. You will learn to analyze the amplifier equivalent circuit and determine the critical frequencies that limit the response at low and high frequencies. You will learn some special techniques to determine these frequencies. BJT and MOSFET amplifiers will be considered. You will also learn the concepts that are pursued to design a wide band width amplifier. Following topics will be considered.

- Review of Bode plot technique.
- Ways to write the transfer (i.e., gain) functions to show frequency dependence.
- Band-width limiting at low frequencies (i.e., DC to f_L). Determination of lower band cut-off frequency for a single-stage amplifier – short circuit time constant technique.
- Band-width limiting at high frequencies for a single-stage amplifier. Determination of upper band cut-off frequency- several alternative techniques.
- Frequency response of a single device (BJT, MOSFET).
- Concepts related to wide-band amplifier design – BJT and MOSFET examples.

3.1 A short review on Bode plot technique

Example: Produce the Bode plots for the magnitude and phase of the transfer function

$T(s) = \dfrac{10s}{(1+s/10^2)(1+s/10^5)}$, for frequencies between 1 rad/sec to 10^6 rad/sec.

We first observe that the function has zeros and poles in the numerical sequence 0 (zero), 10^2 (pole), and 10^5 (pole). Further at ω=1 rad/sec i.e., lot less than the first pole (at ω=10^2 rad/sec), $T(s) \cong 10s$. Hence the first portion of the plot will follow the asymptotic line rising at 6 dB/octave, or 20 dB/decade, in the neighborhood of ω=1 rad/sec. The magnitude of *T(s)* in decibels will be approximately 20 dB at ω= 1 rad/sec.

The second asymptotic line will commence at the pole of $\omega=10^2$ rad/sec, running at -6 dB/octave slope relative to the previous asymptote. Thus the overall asymptote will be a line of slope zero, i.e., a line parallel to the ω- axis.

The third asymptote will commence at the pole $\omega=10^5$ rad/sec, running at -6 dB/Octave slope relative to the previous asymptote. The overall asymptote will be a line dropping off at -6 dB/octave beginning from $\omega=10^5$ rad/sec.

Since we have covered all the poles and zeros, we need not work on sketching any further asymptotes. The three asymptotic lines are now sketched as shown in figure 3.1.

Asymptote
lines

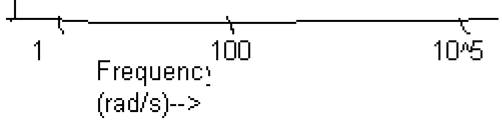


Figure 3.1: The asymptotic line plots for the *T(s)*.

The actual plot will follow the asymptotic lines being 3 dB below the first corner point (i.e.,at ω=100)i.e., 57 dB ,and 3 dB below the second corner point (i.e., ω=10^5), i.e. 57 dB. In between the two corner point the plot will approach the asymptotic line of constant value 60 dB. The magnitude plot is shown in figure 3.2.

Magnitude plot (heavier line)

Figure 3.2:Bode magnitude plot for *T(s)*

For phase plot, we note that the ‘s’ in the numerator will give a constant phase shift of +90^o degrees (since $s \rightarrow j\omega \rightarrow 0 + j\omega$, angle: $\tan^{-1}(\omega/0) \rightarrow \tan^{-1}(\infty) \rightarrow 90^o$), while the terms in the denominator will produce angles of $-\tan^{-1}(\omega/10^2)$, and $-\tan^{-1}(\omega/10^5)$ respectively. The total phase angle will then be:

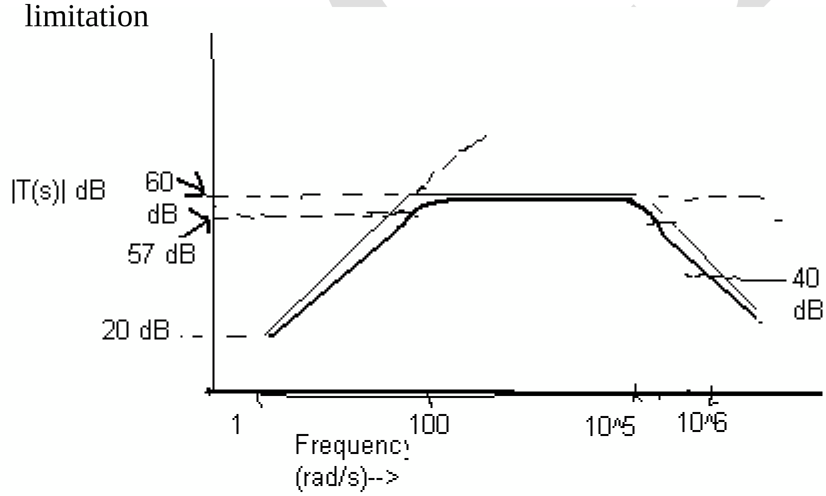
$$\phi(\omega) = 90^o - \tan^{-1}(\omega/10^2) - \tan^{-1}(\omega/10^5) \qquad (3.1)$$

Thus at low frequency (<< 100 rad/sec), the phase angle will be close to 90^o. Near the pole frequency $\omega=100$, a -45^o will be added due to the ploe at making the phase angle to be close to $+45^o$. The phase angle will progressively decrease, because of the first two terms in $\varphi(\omega)$. Near the second pole $\omega=10^5$, the phase angle will approach

$$\phi(\omega) = 90^o - \tan^{-1}(10^5/10^2) - \tan^{-1}(10^5/10^5) \cong 90^o - 90^o - 45^o$$ i.e., -45^o degrees.

(The student in encouraged to draw the curve)

3.2 Simplified form of the gain function of an amplifier revealing the frequency response limitation



3.2.1 Gain function at low frequencies

Electronic amplifiers are limited in frequency response in that the response magnitude falls off from a constant mid-band value to lower values both at frequencies below and above an intermediate range (the mid-band) of frequencies. A typical frequency response curve of an amplifier system appears as in figure3.3.

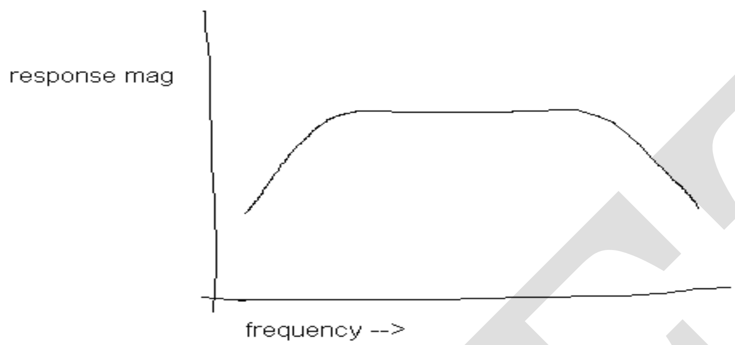


Figure 3.3: Typical frequency response function magnitude plot for an electronic amplifier

Using the concepts of Bode magnitude plot technique, we can approximate the low-frequency portion of the sketch above by an expression of the form $T_L(s) = \frac{Ks}{s+a}$, or $T_L(s) = \frac{K}{1+a/s}$. In this K and a are constants and $s=j\omega$, where ω is the (physical, i.e., measurable) angular frequency (in rad/sec). In either case, when the signal frequency is very much smaller than the pole frequency 'a', the response $T_L(s)$ takes the form Ks/a. This function increases progressively with the frequency $s = j\omega$, following the asymptotic line with a slope of +6 dB per octave. At the pole frequency ‘a’, the response will be 3 dB below the previous asymptotic line, and henceforth follow an asymptotic line of slope (-6+6=0) of zero dB/ octave. Thus $T_L(s)$ will remain constant with frequency, assuming the mid-band value. Note that $T_L(s)$ is a first order function in ‘s’ (a single time-constant function).

The *frequency* at which the magnitude plot reaches *3 dB below the mid-band* (i.e., the flat portion of the magnitude response curve) gain value is known as the *-3 dB frequency* of the gain

Low Frequency Response of a FET Circuit

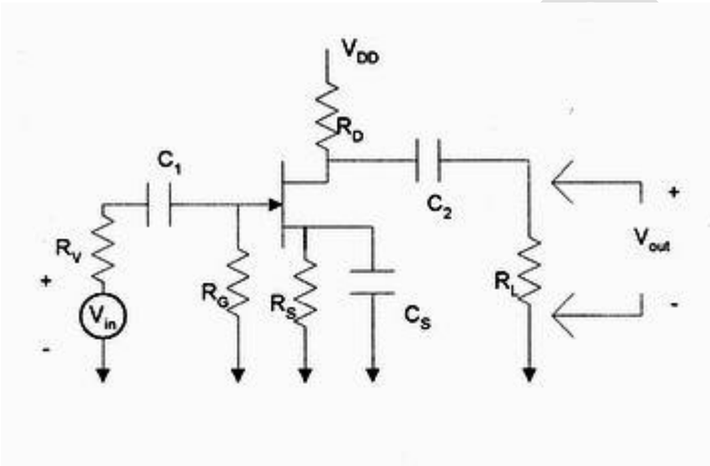


Figure 1

The Field Effect Transistor circuit low frequency response can be evaluated by analyzing the transfer functions of the elements which affect the response at frequencies below midband. If there is more then one transfer function, the resultant overall response can be determined from the product of the individual response; usually done graphically with a Bode plot.

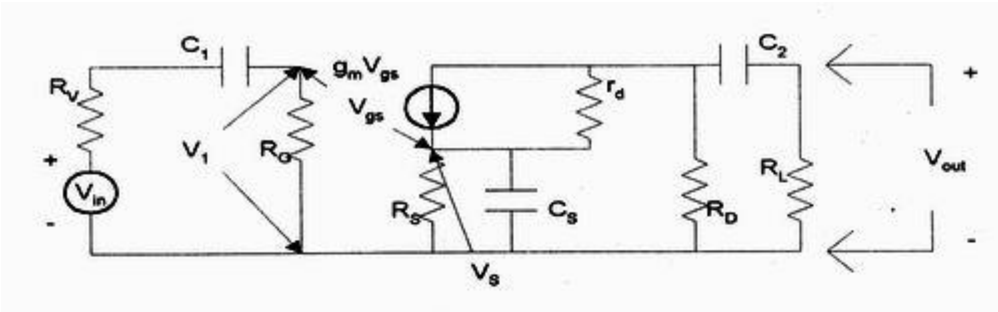


Figure 2

Figure 2 shows the low frequency equivalent of the circuit of the FET configuration in Figure 1. When examining the input circuit, the input transfer function is developed from C_1 , R_G , and R_V.

$V1 = V_{in}R_G / (R_V + R_G) + (1/j\omega C_1)$

$V1 / V_{in} = R_G / R_V + R_G(1 / (1 - j (1 / \omega(R_V + R_G) C)))$

$V1 / V_{in} = R_G / R_V + R_G(1 / (1 - j (\omega_1(\text{input})) / \omega))$

$(R_V + R_G) C = 1 / \omega_1(\text{input}) = 1 / 2 \pi f_1(\text{input})$

Examining this expression reveals a pole in the low frequency response produced by the input elements, C_1 , R_G , and R_V at a frequency of $f_{1(\text{input})} = 1 / 2 \pi (R_V + R_G) C_1$

The output elements of the circuit can also be expected to produce a low frequency pole. Evaluating the affect separately by assuming R_S in parallel with $C_S = Z_S = 0$. And r_d in parallel with $R_D = R$ the following equivalent circuit in Figure 3 can be produced.

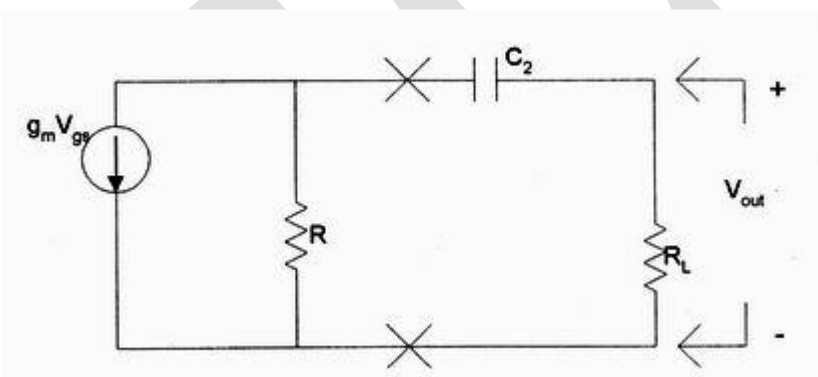


Figure 3

UNIT-3

Multivibrators

Multivibrator

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors orcapacitors. The name "multivibrator" was initially applied to the free-running oscillator version of the circuit because its output waveform was rich in harmonics.[1] There are three types of multivibrator circuits depending on the circuit operation:

- astable, in which the circuit is not stable in either state —it continually switches from one state to the other. It does not require an input such as a clock pulse.
- monostable, in which one of the states is stable, but the other state is unstable (transient). A trigger causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a one shot.
- bistable, in which the circuit is stable in either state. The circuit can be flipped from one state to the other by an external event or trigger.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

History

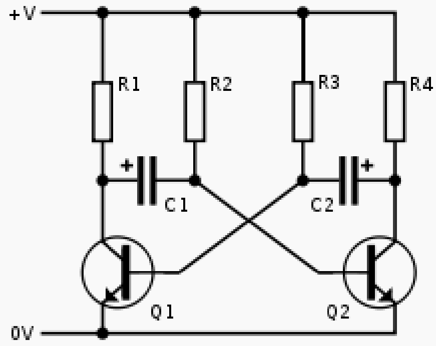
The classic multivibrator circuit (also called a plate-coupled multivibrator) is first described by H. Abraham and E. Bloch in Publication 27 of the French Ministère de la Guerre, and in Annales de Physique 12, 252 (1919). It is a predecessor of Eccles-Jordan trigger[2]derived from this circuit a year later.

Astable multivibrator

An astable multivibrator is a regenerative circuit consisting of two amplifying stages connected in a positive feedback loop by two capacitive-resistive coupling networks. The amplifying elements may be junction or field-effect transistors, vacuum tubes, operational amplifiers, or other types of amplifier. The example diagram shows bipolar junction transistors.

The circuit is usually drawn in a symmetric form as a cross-coupled pair. Two output terminals can be defined at the active devices, which will have complementary states; one will have high voltage while the other has low voltage, (except during the brief transitions from one state to the other).

Operation



1: Basic BJT astable multivibrator

The circuit has two stable states that change alternatively with maximum transition rate because of the "accelerating" positive feedback. It is implemented by the coupling capacitors that instantly transfer voltage changes because the voltage across a capacitor cannot suddenly change. In each state, one transistor is switched on and the other is switched off. Accordingly, one fully charged capacitor discharges (reverse charges) slowly thus converting the time into an exponentially changing voltage. At the same time, the other empty capacitor quickly charges thus restoring its charge (the first capacitor acts as a time-setting capacitor and the second prepares to play this role in the next state). The circuit operation is based on the fact that the forward-biased base-emitter junction of the switched-on bipolar transistor can provide a path for the capacitor restoration.

State 1 (Q1 is switched on, Q2 is switched off):

In the beginning, the capacitor C1 is fully charged (in the previous State 2) to the power supply voltage V with the polarity shown in Figure 1. Q1 is on and connects the left-hand positive plate of C1 to ground. As its right-hand negative plate is connected to Q2 base, a maximum negative voltage (-V) is applied to Q2 base that keeps Q2 firmly off. C1 begins discharging (reverse charging) via the high-resistive base resistor R2, so that the voltage of its right-hand plate (and at the base of Q2) is rising from below ground (-V) toward +V. As Q2 base-emitter junction is backward-biased, it does not impact on the exponential process (R2-C1 integrating network is unloaded). Simultaneously, C2 that is fully discharged and even slightly charged to 0.6 V (in the previous State 2) quickly charges via the low-resistive collector resistor R4 and Q1 forward-biased base-emitter junction (because R4 is less than R2, C2 charges faster than C1). Thus C2 restores its charge and prepares for the next State 2 when it will act as a time-setting capacitor. Q1 is firmly saturated in the beginning by the "forcing" C2 charging current added to R3 current; in the end, only R3 provides the needed input base current. The resistance R3 is chosen small enough to keep Q1 (not deeply) saturated after C2 is fully charged.

When the voltage of C1 right-hand plate (Q2 base voltage) becomes positive and reaches 0.6 V, Q2 base-emitter junction begins diverting a part of R2 charging current. Q2 begins conducting and this starts the avalanche-like positive feedback process as follows. Q2 collector voltage begins falling; this change transfers through the fully charged C2 to Q1 base and Q1 begins cutting off. Its collector voltage begins rising; this change transfers back through the almost empty C1 to Q2 base and makes Q2 conduct more thus sustaining the initial input impact on Q2 base. Thus the initial input change circulates along the feedback loop and grows in an avalanche-like manner until finally Q1 switches off and Q2 switches on. The forward-biased Q2 base-emitter junction fixes the voltage of C1 right-hand plate at 0.6 V and does not allow it to continue rising toward +V.

State 2 (Q1 is switched off, Q2 is switched on):

Now, the capacitor C2 is fully charged (in the previous State 1) to the power supply voltage V with the polarity shown in Figure 1. Q2 ison and connects the right-hand positive plate of C2 to ground. As its left-hand negative plate is connected to Q1 base, a maximum negative voltage (-V) is applied to Q1 base that keeps Q1 firmly off. C2 begins discharging (reverse charging) via the high-resistive base resistor R3, so that the voltage of its left-hand plate (and at the base of Q1) is rising from below ground (-V) toward +V. Simultaneously, C1 that is fully discharged and even slightly charged to 0.6 V (in the previous State 1) quickly charges via the low-resistive collector resistor R1 and Q2 forward-biased base-emitter junction (because R1 is less than R3, C1 charges faster than C2). Thus C1 restores its charge and prepares for the next State 1 when it will act again as a time-setting capacitor...and so on... (the next explanations are a mirror copy of the second part of Step 1).

Multivibrator period (frequency)

Derivation

The duration of state 1 (low output) will be related to the time constant R_2C_1 as it depends on the charging of C1, and the duration of state 2 (high output) will be related to the time constant R_3C_2 as it depends on the charging of C2. Because they do not need to be the same, an asymmetric duty cycle is easily achieved. The extended content below contains a derivation of the multivibrator period (frequency); click the show button to see the content.

The voltage on a capacitor with non-zero initial charge is:

$$V_{\text{cap}}(t) = \left[(V_{\text{capinit}} - V_{\text{charging}}) \times e^{-\frac{t}{RC}}\right] + V_{\text{charging}}$$

Looking at C2, just before Q2 turns on the left terminal of C2 is at the base-emitter voltage of Q1 (V_{BE_Q1}) and the right terminal is atV_{CC} ("V_{CC}" is used here instead of "+V" to ease notation). The voltage across C2 is V_{CC} minus V_{BE_Q1} . The moment after Q2 turns on, the right terminal of C2 is now at 0 V which drives the left terminal of C2 to 0 V minus (V_{CC} - V_{BE_Q1}) or V_{BE_Q1} - V_{CC}. From this instant in time, the left terminal of C2 must be charged back up to V_{BE_Q1}. How long this takes is half our multivibrator switching time (the other half comes from C1). In the charging capacitor equation above, substituting:

V_{BE_Q1} for $V_{\text{cap}}(t)$

(V_{BE_Q1} - V_{CC}) for V_{capinit}

V_{CC} for V_{charging}

results in:

$$V_{\text{BE\_Q1}} = \left([(V_{\text{BE\_Q1}} - V_{\text{CC}}) - V_{\text{CC}}] \times e^{-\frac{t}{RC}}\right) + V_{\text{CC}}$$

Solving for t results in:

$$t = -RC \times \ln\left(\frac{V_{\text{BE\_Q1}} - V_{\text{CC}}}{V_{\text{BE\_Q1}} - 2V_{\text{CC}}}\right)$$

For this circuit to work, $V_{CC} >> V_{BE\_Q1}$ (for example: V_{CC}=5 V, V_{BE_Q1}=0.6 V), therefore the equation can be simplified to:

$$t = -RC \times \ln\left(\frac{-V_{\text{CC}}}{-2V_{\text{CC}}}\right)$$

or

$$t = -RC \times \ln\left(\frac{1}{2}\right)$$

or

$$t = RC \times \ln(2)$$

The period of each half of the multivibrator is therefore given by t = ln(2)RC.

Summary

The total period of oscillation is given by:

$T = t_1 + t_2 = \ln(2)R_2 C_1 + \ln(2)R_3 C_2$

$$f = \frac{1}{T} = \frac{1}{\ln(2) \cdot (R_2C_1 + R_3C_2)} \approx \frac{1}{0.693 \cdot (R_2C_1 + R_3C_2)}$$

where...

- f is frequency in hertz.
- R_2 and R_3 are resistor values in ohms.
- C_1 and C_2 are capacitor values in farads.
- T is the period (In this case, the sum of two period durations).

For the special case where

- $t_1 = t_2$ (50% duty cycle)
- $R_2 = R_3$
- $C_1 = C_2$

$$f = \frac{1}{T} = \frac{1}{\ln(2) \cdot 2RC} \approx \frac{0.721}{RC}$$ [3]

[edit]Output pulse shape

The output voltage has a shape that approximates a square waveform. It is considered below for the transistor Q1.

During State 1, Q2 base-emitter junction is backward-biased and the capacitor C1 is "unhooked" from ground. The output voltage of the switched-on transistor Q1 changes rapidly from high to low since this low-resistive output is loaded by a high impedance load (the series connected capacitor C1 and the high-resistive base resistor R2).

During State 2, Q2 base-emitter junction is forward-biased and the capacitor C1 is "hooked" to ground. The output voltage of the switched-off transistor Q1 changes exponentially from low to high since this relatively high resistive output is loaded by a low impedance load (the capacitance C1). This is the output voltage of R_1C_1 integrating circuit.

To approach the needed square waveform, the collector resistors have to be low resistance. The base resistors have to be low enough to make the transistors saturate in the end of the restoration ($R_B < \beta.R_C$).

Initial power-up

When the circuit is first powered up, neither transistor will be switched on. However, this means that at this stage they will both have high base voltages and therefore a tendency to switch on, and inevitable slight asymmetries will mean that one of the transistors is first to switch on. This will quickly put the circuit into one of the above states, and oscillation will ensue. In practice, oscillation always occurs for practical values of R and C.

However, if the circuit is temporarily held with both bases high, for longer than it takes for both capacitors to charge fully, then the circuit will remain in this stable state, with both bases at 0.6 V, both collectors at 0 V, and both capacitors charged backwards to −0.6 V. This can occur at startup without external intervention, if R and C are both very small.

Frequency divider

An astable multivibrator can be synchronized to an external chain of pulses. A single pair of active devices can be used to divide a reference by a large ratio, however, the stability of the technique is poor owing to the variability of the power supply and the circuit elements; a division ratio of 10, for example, is easy to obtain but not dependable. Chains of bistable flip-flops provide more predictable division, at the cost of more active elements.[3]

Protective components

While not fundamental to circuit operation, diodes connected in series with the base or emitter of the transistors are required to prevent the base-emitter junction being driven into reverse breakdown when the supply voltage is in excess of the V_{eb} breakdown voltage, typically around 5-10 volts for general purpose silicon transistors. In the monostable configuration, only one of the transistors requires protection.

Monostable multivibrator circuit

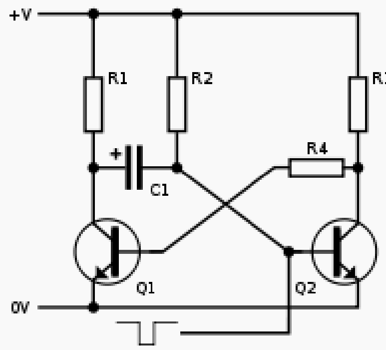


Figure 2: Basic BJT monostable multivibrator.

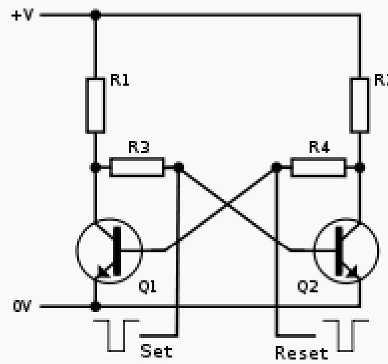


Figure 3: Basic BJT bistable multivibrator (suggested values: R1, R2= 1 kΩ R3, R4 = 10 kΩ).

In the monostable multivibrator, the one resistive-capacitive network (C_2-R_3 in figure 1) is replaced by a resistive network (just a resistor). The circuit can be thought as a 1/2 astable multivibrator. Q2 collector voltage is the output of the circuit (in contrast to the astable circuit, it has a perfect square waveform since the output is not loaded by the capacitor).

When triggered by an input pulse, a monostable multivibrator will switch to its unstable position for a period of time, and then return to its stable state. The time period monostable multivibrator remains in unstable state is given by $t = \ln(2)R_2C_1$. If repeated application of the input pulse maintains the circuit in the unstable state, it is called a retriggerable monostable. If further trigger pulses do not affect the period, the circuit is a non-retriggerable multivibrator.

For the circuit in Figure 2, in the stable state Q1 is turned off and Q2 is turned on. It is triggered by zero or negative input signal applied to Q2 base (with the same success it can be triggered by applying a positive input signal through a resistor to Q1 base). As a result, the circuit goes inState 1 described above. After elapsing the time, it returns to its stable initial state.

Bistable multivibrator circuit

Main article: Flip-flop (electronics)

In the bistable multivibrator, both the resistive-capacitive network are replaced by resistive networks (just resistors or direct coupling).

This latch circuit is similar to an astable multivibrator, except that there is no charge or discharge time, due to the absence of capacitors. Hence, when the circuit is switched on, if Q1 is on, its collector is at 0 V. As a result, Q2 gets switched off. This results in more than half +Vvolts being applied to R4 causing current into the base of Q1, thus keeping it on. Thus, the circuit remains stable in a single state continuously. Similarly, Q2 remains on continuously, if it happens to get switched on first.

Switching of state can be done via Set and Reset terminals connected to the bases. For example, if Q2 is on and Set is grounded momentarily, this switches Q2 off, and makes Q1 on. Thus, Set is used to "set" Q1 on, and Reset is used to "reset" it to off state.

What are multivibrators and what are their types?

Multivibrators is a switching circuit and may be defined as an electronic circuit that generates non-sinusoidal waves such as rectangular waves, sawtooth waves, square waves etc. Multivibrator are capable of storing binary nos, counting pulses, synchronising arithmetic operations and performing other essential functions used in digital systems.

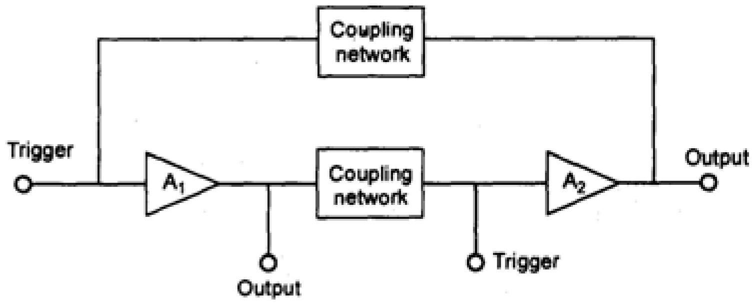
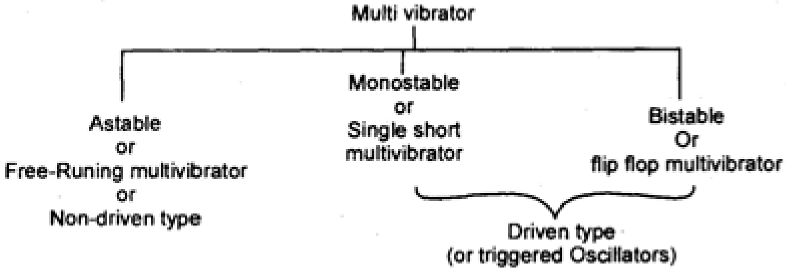


Fig. Basic configuration of a Multivibrator



Uses: 1. Generation of Non-sinusoidal waveform (square, Rectangular sawtooth, etc.)
2. Pulses occurring periodically, frequency division, synchroniseed generation of pulses and extended waveform, generation of time delays, storage of binary bit of information etc.

What are advantages and disadvantages of symmetrical and unsymmetrical Triggering?

Triggering is the process of applying an external signal to induce transition from one state to another. The signal used for triggering is either a pulse of short duration or a step voltage. There are two processes of triggering i.e. unsymmetrical triggering and symmetrical triggering.

Unsymmetrical triggering is a process in which the signal is effective in inducing transition only in one direction. If reverse transition is to be introduced, a second triggering signal from a separate source has to be introduced in a different manner.

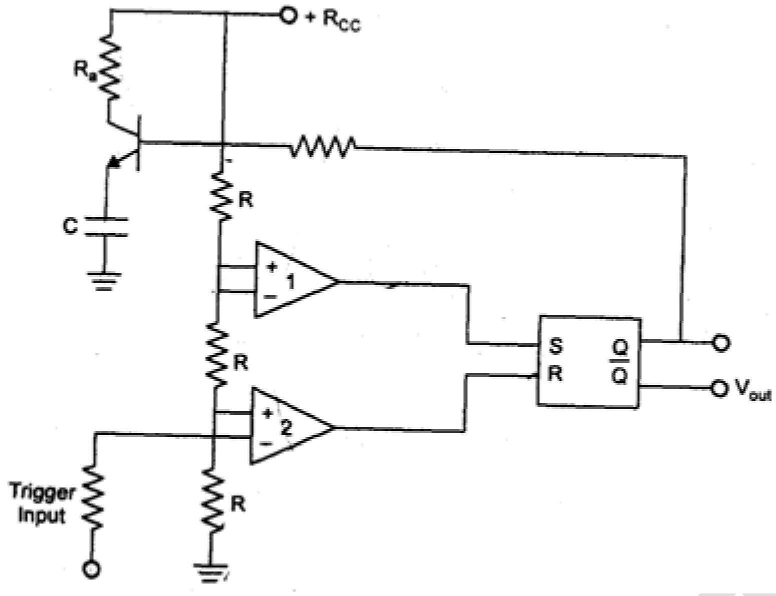
Symmetrical triggering is a process in which each successive triggering signal induces a transition, regardless of the state in which the binary happens to be. Thus, symmetrical triggering requires one source to produce transition whereas in unsymmetrical triggering, two separate sources are required.

Triggering signals may be applied at the output of a stage or the input of a stage.

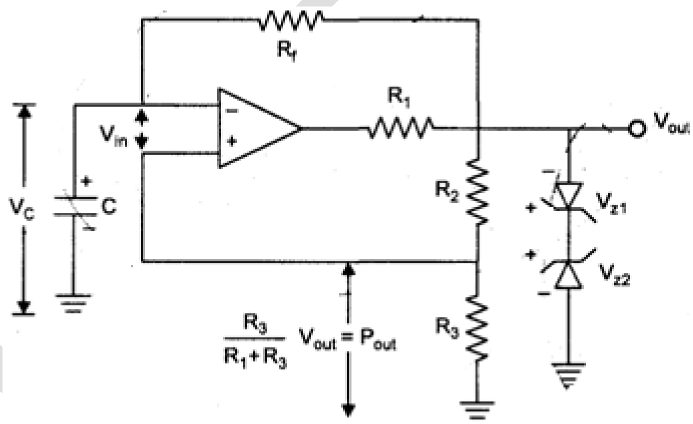
In case of transistors, these signals may be applied at the collector or at the base of the transistor. Symmetrical triggering is used in binary counting circuits and in other applications.

Unsymmetrical triggering is used in logic circuitry (in electronic registers, coding etc.) and is also used as a generator of a gate whose width equals the interval between triggers.

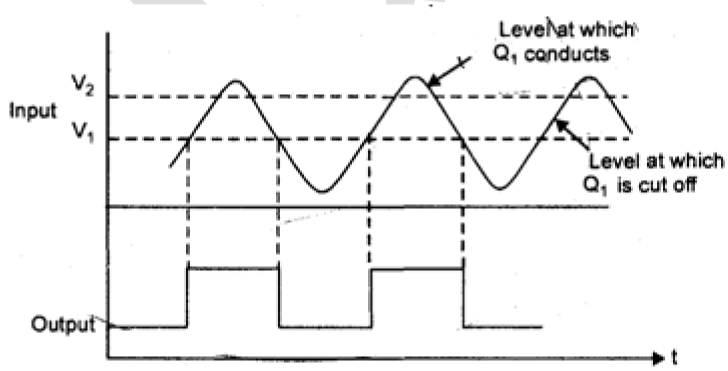
Design monostable multivibrator using OP-AMP.



Sketch the circuit of OP-AMP astable multivibrators.



Sketch typical input/output characteristics for a schmitt trigger circuit.



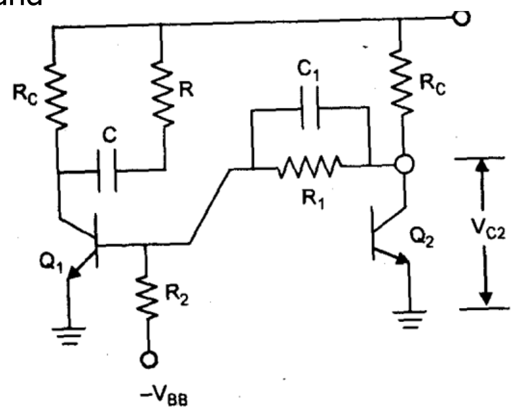
Show that gate width of a collector coupled monostable multivibrator is 0.69 RC.

Ans. The gate width T is given by

$$T = Z.\log_e \frac{V_{YY} + I_1 R_Y - V_T}{V_{YY} - V_Y}$$

... (1)

Where T is gate time, and $V_\sigma = V_{BE(sat)}$



Collector coupled NPN Transistor Monostable multivibrator.
Vt is forward biased voltage 0.1 V for Ge and 0.5V for Si.
The value of T can be made almost independent of transistor characteristics supply voltages and resistance value of Q_1 is driven in saturation. Under such conditions

$$I_1 R_C = V_{CC} - V_{CE}(sat.)$$

Since $V_\sigma = B_{BE(sat)}$; then from eq. (1)

$$T = Z.\log_e \left[\frac{2V_{CC} - V_{CC}(sat) - V_{BE}(sat)}{V_{CC} - V_Y} \right]$$

$$= Z.\log_e \left[\frac{V_{CC} - \frac{V_{CE}(sat) + V_{BE}(sat)}{2}}{V_{CC} - V_Y} \right]$$

... (2)

At room temperature

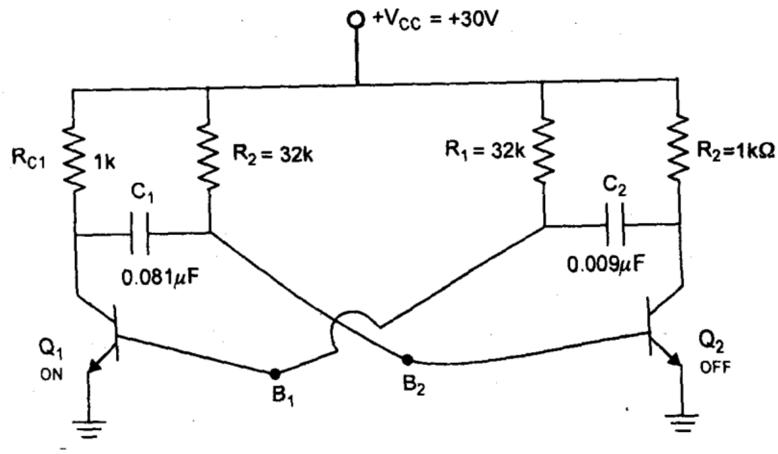
$$V_{CE}(sat) + V_{BE}(sat) \cong 2V_Y$$

and T= 2 $\log_e$ Z= 0.693(R+R_{out}) C
T=0.693 RC

as R_{out} is small for transistor in saturation.

Design an astable multivibrator the repetition rate is 500 Hz and pulse width is 0.2 ms. Use two transistors with h_{fe} = 50, V_{CC} = V_{BB} = 20V RC_1 = RC_2 = 1 K.

Ans.



Collector resistances

$$R_{C1} = R_{C2} = 1K\Omega$$

Repetition rate, $f = 500$ Hz

Pulse width, $P_w = 0.2$ ms

h_{fe} of transistors = 50

$$V_{CC} = V_{BB} = 20V$$

Let the junction voltages be

$$V_{CE(sat)} = 0.3V \text{ and } V_{BE(sat)} = 0.7V$$

$$I_{CE(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{20-0.3}{1K\Omega} = 20mA.$$

Base current, I_B (min) $= \frac{I_{C(sat)}}{R_C} = \frac{20-0.3}{1K\Omega} = 0.4$ mA

Let us take I_B (actual) 1.5 times I_B (min) = 1.5 x 0.4 mA =0.6 mA

Let us assume that the transistor are driven equally into saturation during their conducting period

$\therefore$ $R_1 = R_2 = R$

And

$$R = \frac{V_{BB(sat)} - V_{BE(sat)}}{I_B} = \frac{20-0.7}{0.6mA} = 32K\Omega$$

Time period, $T = \frac{1}{f} = \frac{1}{500} = 2$ ms

Duty cycle $\frac{\text{Pulse width}}{T} = \frac{0.2}{2} = 0.1$

$\therefore$ T_2 =0.1T0.1 x2ms=0.2ms

and T_1 =T-T2=2-0.2=1.8ms

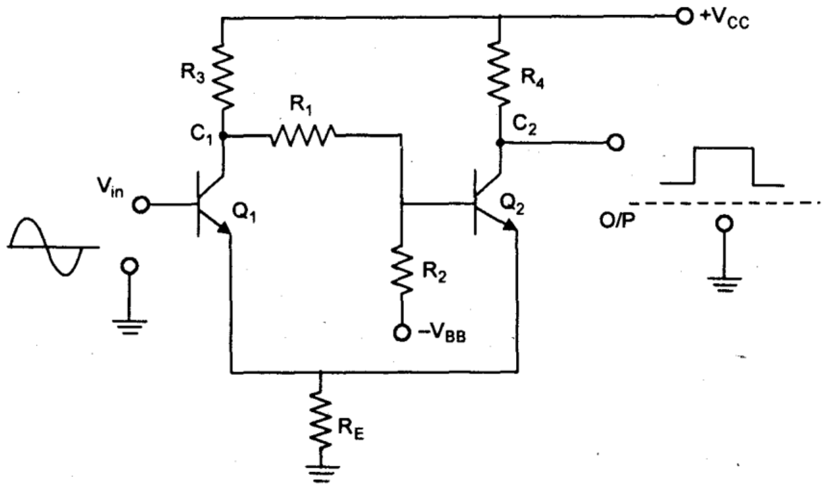
$\therefore$ $\frac{T_2}{T} = 0.1$

$$C_1 = \frac{T_1}{0.693R_2} = \frac{1.8\times10^{-3}}{0.693\times32\times10^3} = 0.081\ \mu F$$

and

$$C_2 = \frac{T_2}{0.693R_1} = \frac{0.2\times10^{-3}}{0.693\times32\times10^3} = 0.009\ \mu F.$$

With the help of basic circuit diagram, discuss the working of a Schmitt Trigger circuit.



It forms an important Bistable multivibrator. It is basically emitter coupled binary oscillator. It has 2 bistable states and V_{in} determines which of the two bistables states is possible. It is preferred in applications where free base terminal is required because here base of transistor Q_1 is not involved in regenerative switching and the base of Q_1 is thus free.

When Q_2 is ON, Q is OFF, $V_{C1} = V_{CC}$ appears across $V_{BE}Q_2$ through C_1 and R_1 and drives Q_2 into saturation and holds it there. Potential divider circuit is through R_3, through R_1 and through R_2.

When V_{in} is high, Q_1 overcomes reverse bias across R_E and makes Q_1 forward biased and V_{C1} drops below and starts decreasing and it reduces forward biased of Q_2 through C_1, R_1 and then R_2 and this decreases I_{E2} and V_{RE} also decreases and reverse bias of Q_1 decreases and Q_1 starts conducting and V_{CQ_1} decreases and Q_2 is cut off and ultimately Q_1 goes into saturation and Q_2 to cut-off.

After half cycle, V_{BQ_1} decreases and Q_1 is reverse biased and I_{C1} decreases, V_{C1} increases, Q_2 is forward biased I_{E2} increases, V_{RE} increases, and Q_1 is reverse biased and ultimately Q_2 goes into saturation and Q_1 is cut-off.

The time period of astable-multivibrator is given by

$$T = 2R_b.\ln\left[1+\left[\frac{V_{bb}}{V_{cc}}\right]\right]$$

Show variation of 'T' by varying V_{bb}. Is the variation linear?

Ans. Time period of Astable multivibrator is given by.

$$T = 2R_b.C.l_n\left[1+\frac{V_{BB}}{V_{CC}}\right] \quad ...(1)$$

From equation (1), it is inferred that the time period T can be varied by varying V_{BB} of course, this variation is not linear.

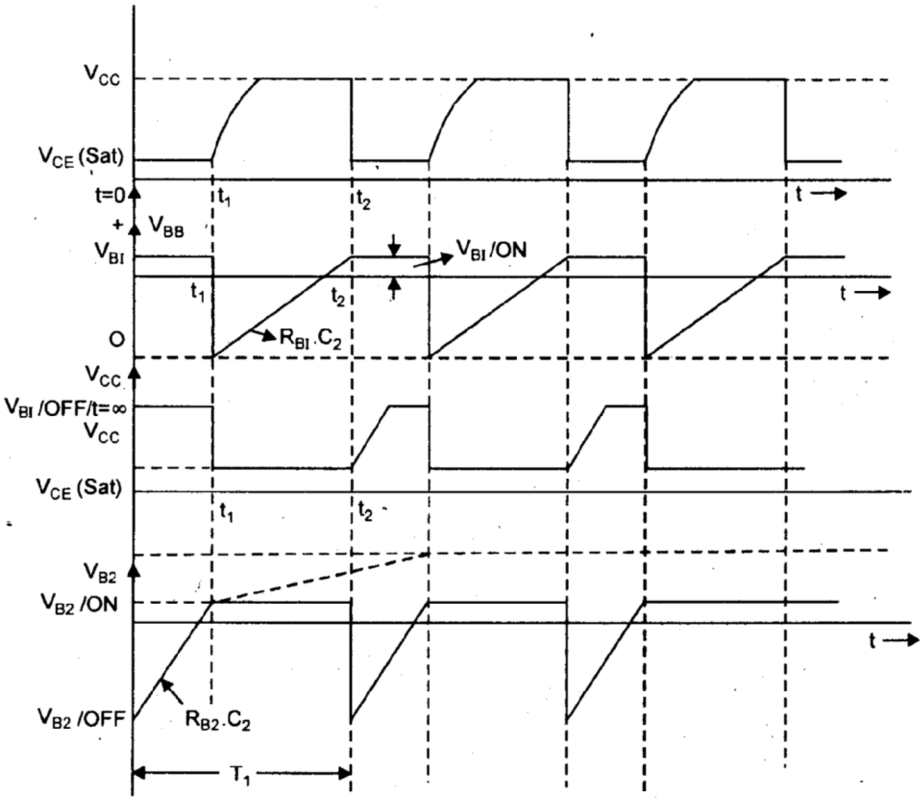


Fig. 1. Collector and base voltage waveform in Astable multivibrator

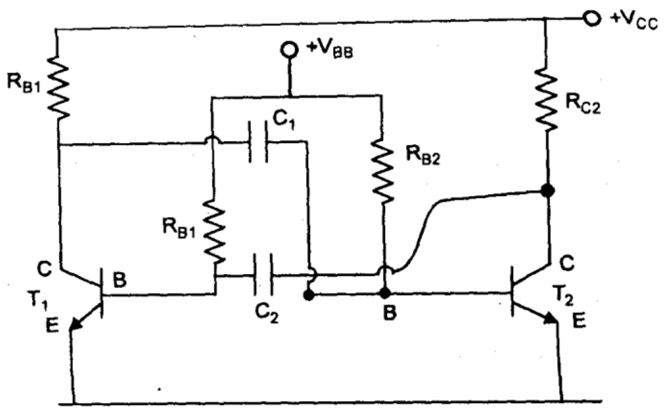
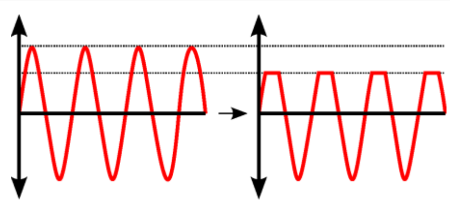


Fig. Astable multivibrator.

<u>Non-Linear Wave Shaping</u>

Clipper

In electronics, a clipper is a device designed to prevent the output of a circuit from exceeding a predetermined voltage level without distorting the remaining part of the applied waveform.



Voltage clipping limits the voltage to a device without affecting the rest of the waveform

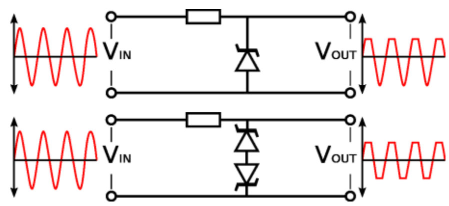
A clipping circuit consists of linear elements like resistors and non-linear elements like junction diodes or transistors, but it does not contain energy-storage elements like capacitors. Clipping circuits are used to select for purposes of transmission, that part of a signal wave form which lies above or below a certain reference voltage level.

Thus a clipper circuit can remove certain portions of an arbitrary waveform near the positive or negative peaks. Clipping may be achieved either at one level or two levels. Usually under the section of clipping, there is a change brought about in the wave shape of the signal.

Clipping Circuits are also called as Slicers, amplitude selectors or limiters. Using square waveform it is easier to analyze the clipper network than sinusoidal waveform,because in square waveform only two level (i.e.two DC level) have to be considered.

Types

Zener Diode



Two shunt diode clipper circuits

In the example circuits above, one or two zener diodes are used to clip the voltage V_{IN}. In the first circuit, the voltage is clipped to the reverse breakdown voltage of the zener diode. The output voltage in the first circuit should also never be more negative than the diode's forward voltage (such as .7V for a typical diode), but it is not shown in the picture. In the second, the voltage in either direction is limited to the reverse breakdown voltage plus the voltage drop across one zener diode.

Classification

Clippers may be classified into two types based on the positioning of the diode.

- Series Clippers, where the diode is in series with the load resistance, and
- Shunt Clippers, where the diode in shunted across the load resistance.

The diode capacitance affects the operation of the clipper at high frequency and influences the choice between the above two types. High frequency signals are attenuated in the shunt clipper as the diode capacitance provides an alternative path to output current. In the series clipper, clipping effectiveness is reduced for the same reason as the high frequency current passes through without being sufficiently blocked.

Clippers may be classified based on the orientation(s) of the diode. The orientation decides which half cycle is affected by the clipping action.

The clipping action can be made to happen at an arbitrary level by using a biasing elements (potential sources) in series with the diode.

- Positively Biased Diode Clipper
- Negatively Biased Diode Clipper

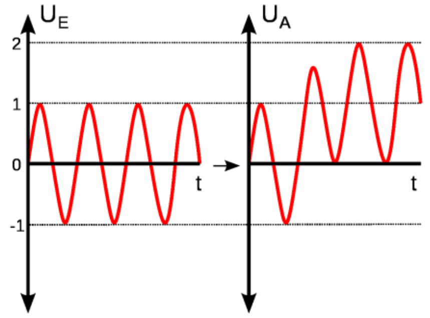
The signal can be clipped to between two levels by using both types of diode clippers in combination. [2] This clipper is referred to as

- Combinational Diode Clipper or Two-Level Clippers

The clamping network is the one that will "clamp" a signal to a different dc level. The network must have capacitor, a diode, and a resistive element, but it also employs an independent dc supply to introduce an additional shift.

Clamper (electronics)

A clamper is an electronic circuit that prevents a signal from exceeding a certain defined magnitude by shifting its DC value. The clamper does not restrict the peak-to-peak excursion of the signal, but moves it up or down by a fixed value. A diode clamp (a simple, common type) relies on a diode, which conducts electric current in only one direction; resistors and capacitors in the circuit are used to maintain an altered DC level at the clamper output.



Positive unbiased voltage clamping shifts the amplitude of the input waveform so that all parts of it are greater than 0 V

General function

A clamping circuit (also known as a clamper) will bind the upper or lower extreme of a waveform to a fixed DC voltage level. These circuits are also known as DC voltage restorers. Clampers can be constructed in both positive and negative polarities. When unbiased, clamping circuits will fix the voltage lower limit (or upper limit, in the case of negative clampers) to 0 Volts. These circuits clamp a peak of a waveform to a specific DC level compared with a capacitively coupled signal which swings about its average DC level.

Types

Clamp circuits are categorised by their operation; negative or positive, and biased or unbiased. A positive clamp circuit outputs a purely positive waveform from an input signal; it offsets the input signal so that all of the waveform is greater than 0 V. A negative clamp is the opposite of this - this clamp outputs a purely negative waveform from an input signal.

A bias voltage between the diode and ground offsets the output voltage by that amount.

For example, an input signal of peak value 5 V (V_{IN} = 5 V) is applied to a positive clamp with a bias of 3 V (V_{BIAS} = 3 V), the peak output voltage will be

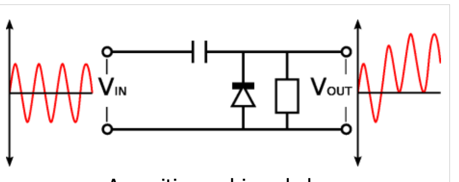
$$V_{OUT} = 2V_{IN} + V_{BIAS}$$

$V_{OUT} = 2 * 5\ V + 3$

$V\ V_{OUT} = 13\ V$

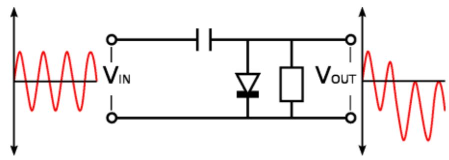
Positive unbiased

In the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of V_{IN}. During the positive cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage gain, so $V_{OUT} = 2V_{IN}$



A positive unbiased clamp

Negative unbiased

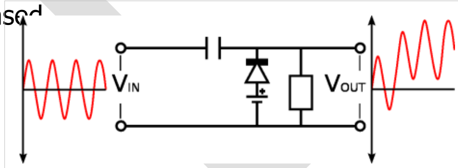


A negative unbiased clamp

A negative unbiased clamp is the opposite of the equivalent positive clamp. In the positive cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak value of V_{IN}. During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage again, so $V_{OUT} = -2V_{IN}$

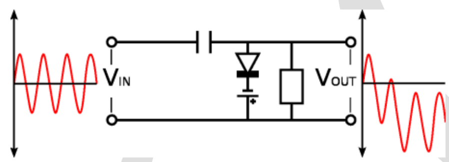
Positive biased

A positive biased voltage clamp is identical to an equivalent unbiased clamp but with the output voltage offset by the bias amount V_{BIAS}. Thus, $V_{OUT} = 2V_{IN} + V_{BIAS}$



A positive biased clamp

Negative biased

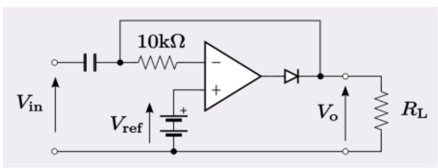


A negative biased clamp

A negative biased voltage clamp is likewise identical to an equivalent unbiased clamp but with the output voltage offset in the negative direction by the bias amount V_{BIAS}. Thus, $V_{OUT} = -2V_{IN} - V_{BIAS}$

Op-amp circuit

The figure shows an op-amp clamp circuit with a non-zero reference clamping voltage. The advantage here is that the clamping level is at precisely the reference voltage. There is no need to take into account the forward volt drop of the diode (which is necessary in the preceding simple circuits as this adds to the reference voltage). The effect of the diode volt drop on the circuit output will be divided down by the gain of the amplifier, resulting in an insignificant error.



Precision op-amp clamp circuit[1]

Clamping for input protection

Clamping can be used to adapt an input signal to a device that cannot make use of or may be damaged by the signal range of the original input.

Principles of operation

The schematic of a clamper reveals that it is a relatively simple device. The two components creating the clamping effect are a capacitor, followed by a diode in parallel with the load. The clamper circuit relies on a change in the capacitor's time constant; this is the result of the diode changing current path with the changing input voltage. The magnitud$\tau = RC$ and C are chosen so that is large enough to ensure that the voltage across the capacitor does

not discharge significantly during the diode's "Non conducting" interval. During the first negative phase of the AC
input voltage, the capacitor in the positive clamper charges rapidly. As V_{in} becomes positive, the capacitor serves as
a voltage doubler; since it has stored the equivalent of V_{in} during the negative cycle, it provides nearly that voltage

during the positive cycle; this essentially doubles the voltage seen by the load. As V_{in} becomes negative, the
capacitor acts as a battery of the same voltage of V_{in}. The voltage source and the capacitor counteract each other,
resulting in a net voltage of zero as seen by the load.

Biasedversus non-biased

By using a voltage source and resistor, the clamper can be biased to bind the output voltage to a different value. The voltage supplied to the potentiometer will be equal to the offset from zero (assuming an ideal diode) in the case of either a positive or negative clamper (the clamper type will determine the direction of the offset. If a negative voltage is supplied to either positive or negative, the waveform will cross the x-axis and be bound to a value of this magnitude on the opposite side. Zener diodes can also be used in place of a voltage source and potentiometer, hence setting the offset at the Zener voltage.

One common such clamping circuit is the DC restorer circuit in analog television receiver, which returns the voltage of the signal during the back porch of the line blanking period to 0 V. Since the back porch is required to be at 0 V on transmission, any DC or low frequency hum that has been induced onto the signal can be effectively removed via this method.

Define short circuit current gain in a wide band amplifier.

Ans. short circuit current gain or f_T parameter of transistor: it is the another high frequency characteristics of a transistor and is define as the frequency at which the common emitter current gain, β falls to unity.

It is related to F_β as

$$f_T = B. f_\beta \quad \text{... (1)}$$

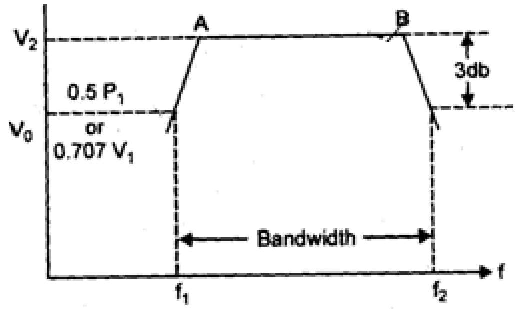
Where β refers to its low frequency value. Obviously f_T is much larger then F_β. However it is smaller than f_α and is related with f_α by the following relation.

$$f_\alpha = 1.2\, f_T \quad \text{... (2)}$$

Define bandwidth, a differentiation and ideal integrator.

Ans. Bandwidth: The difference between the upper cut-off frequency f_2 and lower cut-off frequency f_1 is called the bandwidth -:

$$B.W. = f_2 - f_1$$



Ideal differentiation: An Ideal differentiator circuit in Fig 1. Operator on a given input signal and produces an output which time is derivative of the input signal mathematically then,

$$V_0 = \frac{dv_i}{dt} \quad \ldots (1)$$

In the operational notation equation (1) may be put as,

$$V_0(s) = V_i(s)\ s \quad \ldots (2)$$

Fig. 2 given the gain versus frequency plots of an ideal differentiator.

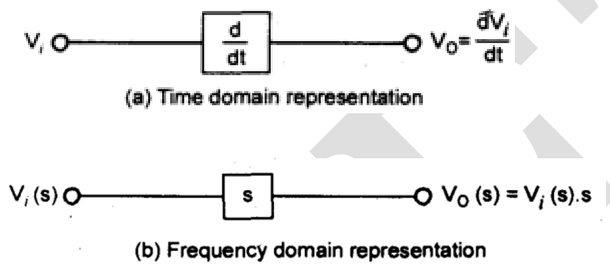


Fig. 1. Time domain and frequency domain representation of an ideal differentiator.

Such an ideal differentiator is physically not realizable since it does not fulfill the necessary conditions for Paley Wiener criterion of physical realizability. The necessary and sufficient condition as per Paley Wiener criterion is,

$$\int_{-\infty}^{+\infty} H|(w)|^2\, dw < \infty \quad \ldots (3)$$

Here, I H (w). Is the modulus of transfer function to be realized.

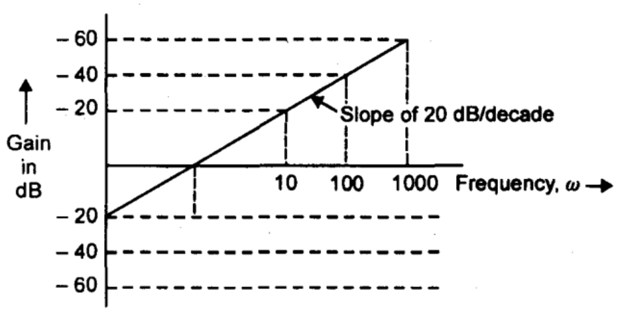
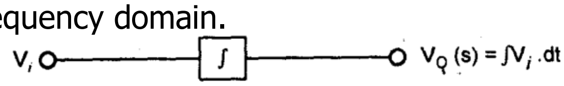
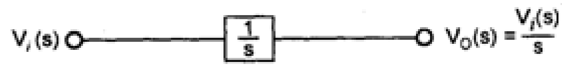


Fig. 2. dB gain versus frequency plot of an ideal differentiator.

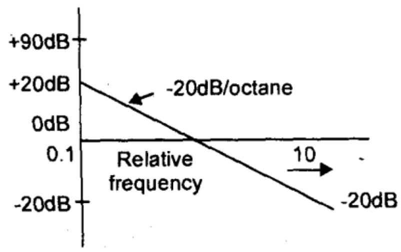
Ideal integrator: An Ideal integrator is one which gives the output voltage as the imegral of the input voltage. Fig.3 shown the symbol of An Ideal integrator in time domain while fig.4 shows the symbol in frequency domain.



(a) Time domain representation of an integrator



(b) Frequency domain representation of an integrator



(c)Gain versus frequency Plot

Fig.3. Ideal integrator

Fig. 3(c) shows the gain frequency plot of an ideal integrator. It may be seen that an ideal integrator has infinite gain for zero frequency i.e. for dc signal further as the frequency increases, the gain falls at the rate of 20 db/ decade.

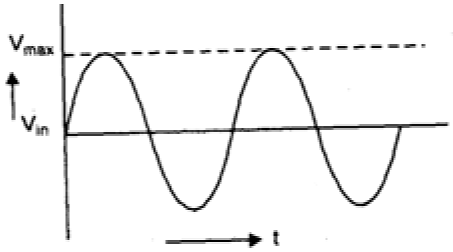
If a sinusoidal voltage. (A sin wt) is passed through an integrator, we get $\left[\frac{A}{w}.\cos wt\right]$ at the output. It may thus be seen that the output has phase-shift of $90°$ and gain of $\left[\frac{1}{w}\right]$. Thus, higher the frequency more is the attenuation. For d.c. signal, this Circuit has infinite gain.

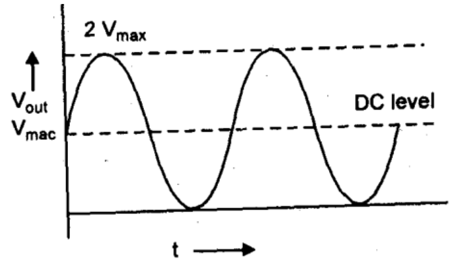
An ideal integrator is physically unrealizable due to the requirement of infinite gain at zero frequency. A practical difficulty in the realization of ideal integrator circuit is the drift associated with high gain d.c. amplifiers.

Discuss briefly working of a practical clamping circuit.

Ans. A circuit that places either the positive or negative peak of a signal at a desired level is known as clamping circuit. It simply adds on subtracts a dc component to the input signal. The clamper is also referred to as a dc restorer and a signal level shifter.

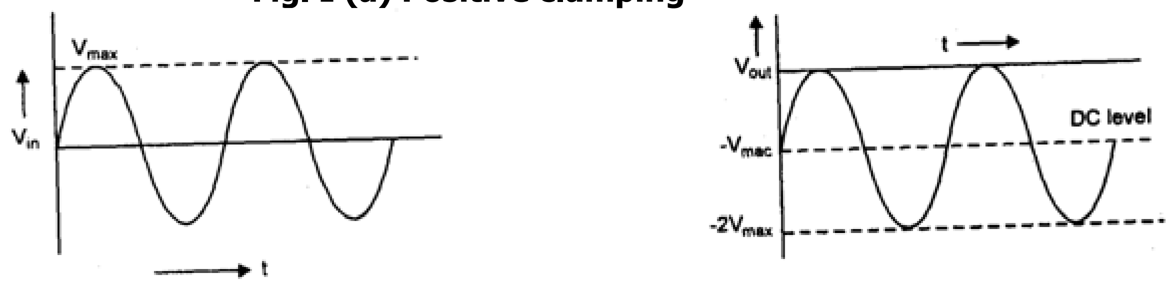
In fact, a clamp circuit adds dc component (positive or negative) to the input signal, so as to push it either on the positive side or on the negative side when the circuit pushes the signal on the (positive) side or upward, the negative peak of the signal coincides with the zero level and the circuit is called the (positive) damper. On the other hand, when the signal is pushed on the negative side or downward, the positive peak of the input signal coincider with the zero level and the circuit is called the negative clamper.





Input signal **Output waveform**

Fig. I (a) Positive clamping



Input signal **Output waveform**

Fig. I (b) Negative clamping.

For a clamping circuit, at least three components—a diode, a capacitor and a resistor are required. Sometimes, an independent dc supply is also required to cause an additional shift.

The important points regarding clamping circuits are:

(1). Waveform remains the same but its level is shifted either upward or downward.

(2). The clamping circuit does not change the peak-to-peak or rms value of the waveform. Thus, referring to fig (1), the input waveform and output waveform have the same peak to peak value i.e. ($2V_{max}$). If the Input voltage and clamped output are measured by an ac voltmeter, the readings will be the same.

(3). The clamping circuit of course, alters the peak and average values of the waveform. In fig. (1), the input waveform has a peak value of V_{max} and average value over a complete cycle is zero. The clamped output varies from $2V_{max}$ and 0 (or 0 and $2V_{max}$) Thus, the peak value of the clamped output is $2V_{max}$ and average value is V_{max}.

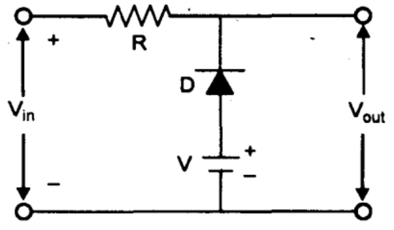
(4). Both resistor R and C offer the waveform.

(5). The value of R and C should be taken such that the time constant of the circuit τ = RC is large enough to ensure that the voltage across the capacitor C does not change significantly during the interval the diode is non-conducting. For good clamping action, the circuit time constant τ = RC should be at least ten times the time period of the input signal voltage.

Explain comparator circuit and its uses.

Ans. A circuit used to mark the instant when an arbitrary waveform attains some particular reference level is called a comparator.

A simple diode comparator circuit is shown is fig (1).



Comparators are of two types, viz non-regenerative type and regenerative type.

Clipping circuits are example of non-regenerative comparators. Blocking oscillators, Schmilt trigger circuits are example of regenerative comparators in which a positive feedback is employed to have an infinite forward gain (unity loop gain).

Application of comparators

(1). Phase meters
(2). Pulse time modulation
(3).Accurate measurement of time
(4). Timing markers generated from a sinusoidal wave
(5). Amplitude distribution analyzers

Why response of an amplifier does not remain flat at all frequencies?

Ans. The fall of in amplifier gain at low frequency due to the effect of coupling and bypass capacitors. At high frequency, the capacitive reactance X_C being equal to $\frac{1}{2\pi f C}$, is very small and therefore all coupling and bypass capacitors behave as short circuit. At low frequencies, capacitive reactance of capacitors X_C increase and some of the signal voltage is lost across the capacitors. Thus, with the decrease in frequency, the reactance of capacitor increases, and therefore, gain of the circuit is fall.

All transistors have capacitances between their terminals. As in fig (2), are so a capacitances C_S .Which are capacitances between wiring and ground these capacitances are very small and therefore at low and medium frequencies are very high. With the increase in frequency, the reactance of stray capacitances FaIl and when these reactance's become small enough, they begin to, shunt away some of the input and output currents. With the increase in frequency, current gain continues to decrease until it become too small to be use.

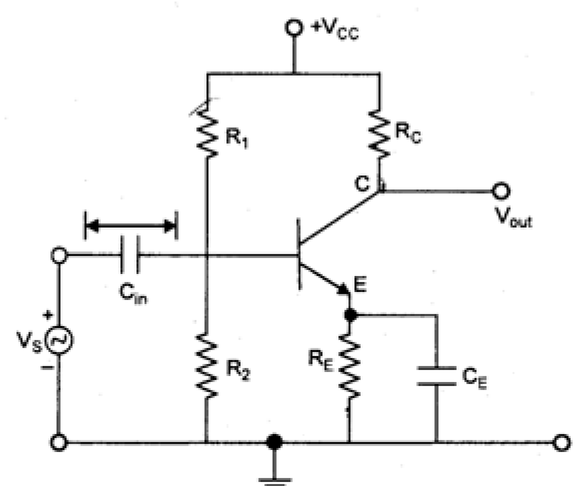


Fig.1 Loss of signal voltage across coupling and Bypass Capacitors at low frequency

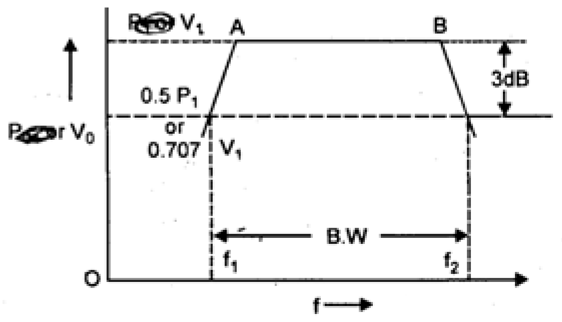


Fig. 2

List two uses of clamping circuit.

Ans. (1) In television receiver or dc resistors.
(2) Storage counter analog frequency meter.
(3) Capacitance meter.
(4) Divider and staircase waveform generator.

What are sweep generators? List the applications.

Ans. Most of the CR0 applications involves measurement or display of a quantity which varies with respect to time. This requires that the CRT (i.e. Cathode Ray Tube) spot moves across the screen with a constant velocity. For this, a voltage which varies linearly with time has to be applied to one set of deflection plates. This voltage is used to sweep the electrons beam across the screen so it is called a sweep voltage. Because of its shape, it is also sometimes called a sawtooth or ramp voltage. The circuits which develop these linearly varying voltages are called time base generators or sweep generator.
Application: Radar and television, indicators, computer monitors, automatic control system, A/D converters

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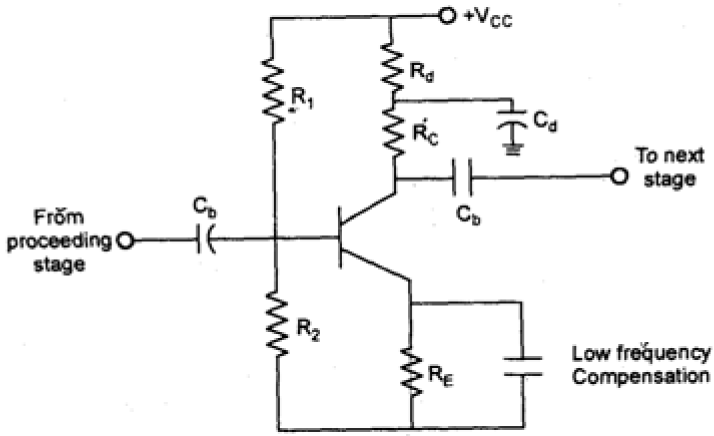
Elaborate the term "low frequency compensation""in amplifier".

Ans.



The amplifier response exhibits a downward tilt at low frequencies due the coupling capacitors. We may compensate such tilt by adding a high resistance R_d is series with R_C the resistance R_d connects to the supply voltage and it is bypass to the ground with large capacitance as C_d shown in figure above.

Explain the term "distributer amplifier".

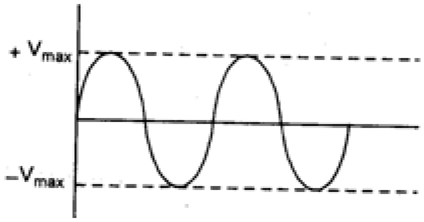
Ans. These amplifiers are useful with vacuum tubes and result in a gain over a bandwidth. Which exceeds the bandwidth attainable with conventional tube amplifiers such amplifiers make use of lumped circuit delay line and so are called the distributer amplifiers.

What is clipping circuit? Give various configurations of clipping circuit.

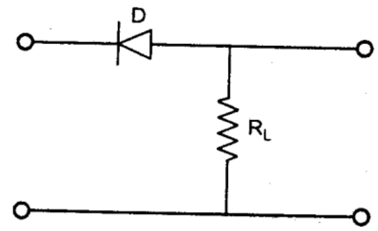
Ans. A wave shaping circuit which controls the shape of the output wave form by removing or clipping a portion of the input wave is known as clipping circuit. Various configurations of clipping circuit are:
(1) Series diode clippers.
(2) Parallel or shunt diode clippers.
(3) A series combination of diode, resistor and reference supply.
(4) Multi-diode clippers consisting of several diodes, resistors and reference voltages.
(5) Two emitter coupled transistors operating as over driven difference amplifier.

The shape of the output waveform by removing or clipping a portion of the input wave is known as the clipping circuit.

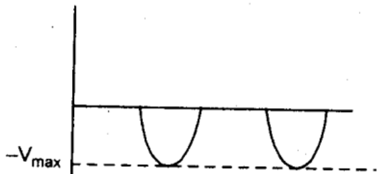
Positive clipper: The clipper which removes the positive half cycle of the input voltage is called the positive clipper.



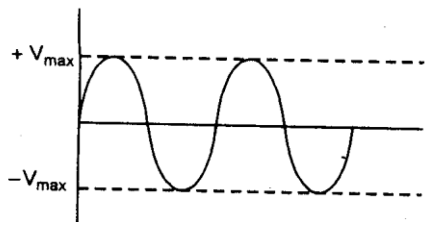
Input waveform

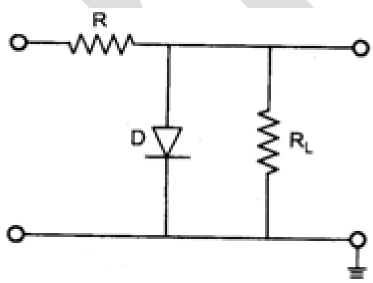


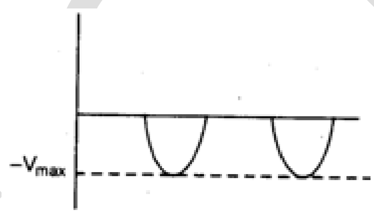
Positive Clipper



Output waveform

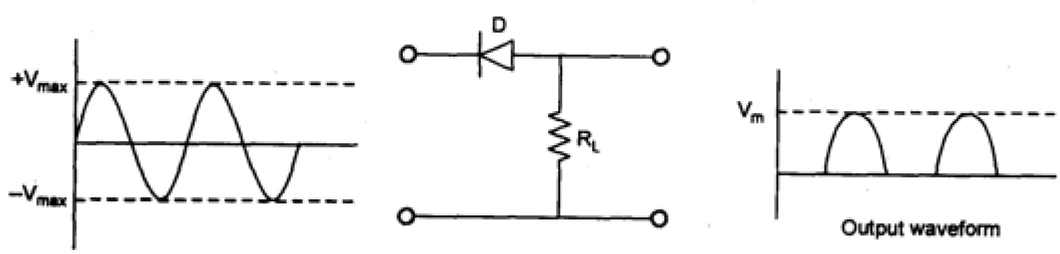




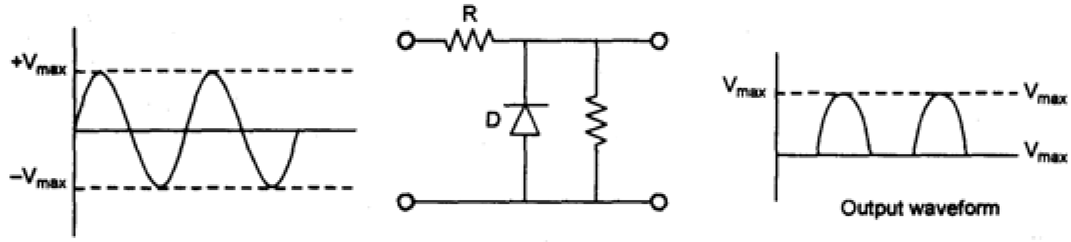


Output waveform

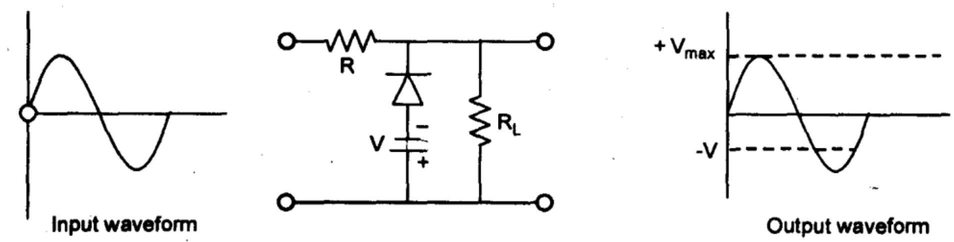
Note: If the diode in above fig reconnected with reversed polarity the circuit will become for a negative series clipper and negative shunt clipper respectively



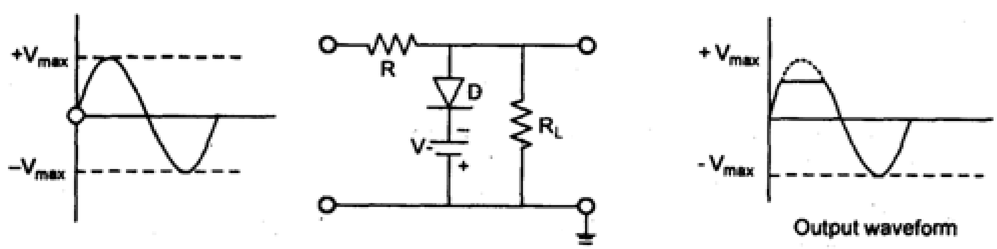
(a) Negative series Clipper



Biased Clipper: Sometimes it is desired to remove a small portion of positive or negative half cycle of the signal voltage. Biased clippers are employed for this purpose

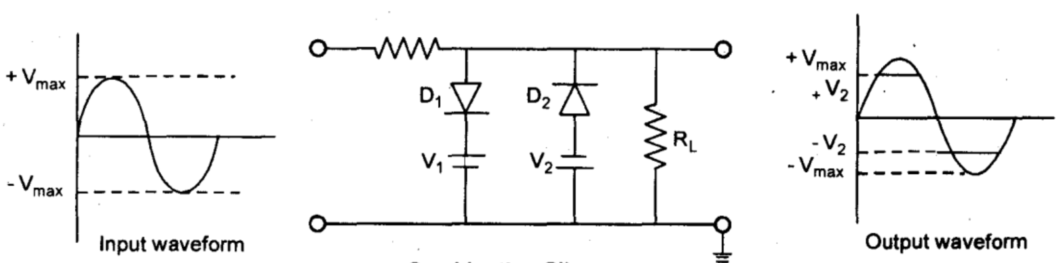


(a) Biased Negative Clipper



(b) Biased positive clipper

Combination Clipper: When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed) combination clipper is employed. The circuit for such a clipper is given in figure.



Combination Clipper

List applications for voltage and current sweep generators.

Ans. Applications of voltage sweep generator: It is used to generate a voltage linearly varying with time and are used, where electrostatic deflection is used such as is CR0.
Current sweep generator: It is used to generate a current varying linearly with time and this current is used to flow through inductors or deflection coils. Current time base generators are used where electromagnetic deflection is used such as in RADARS, TVs etc.

List the applications of clipping circuits.

Ans. Refer Q. No. 10.
Clipping circuits are used in radar, digital computers and other electronic system for removing unwanted portions of the input signal voltages above or below a specified level. Another application is in radio receivers for communication circuits where noise pulses, that rise well above the signal amplitude in clipped down to the desired level.

UNIT-4

UNIT- IV

LINEAR WAVE SHAPING

Timing circuits networks composed of resistors, capacitors and inductors are called linear network and they do not change the waveform of a sine wave when it is transmitted through them. On the other hand when non-sinusoidal waveforms, (e.g. step, ramp, exponential) are applied to the input of such networks the output signal may have very little resembles with the input waveform. The action of a linear network in producing a waveform at its output different from its input is called linear wave shaping. The wave shaping is used to perform any one of the following functions.

1. To hold the waveform to a particular d.c. level.
2. To generate one wave form the other
3. To limit the voltage level of the waveform of some presenting value and suppressing all other voltage levels in excess of the present level.
4. To cut-off the positive and negative portions of the input waveform.

Shaping circuits may be either series RC or series RL circuits. The series RC and RL circuits electrically perform the mathematical operation of integration and differentiation. Therefore, the circuits used to perform these operations are called integrators and differentiator. The differentiator circuits are used to generate sharp narrow pulses either from distorted pulse waveform or from rectangular wave forms. The integrator circuits are required to generate a voltage, which are required to generate a voltage, which increases or decreases linearly with time.

Non-sinusoidal Waveforms

Any waveform whose shape is different from that of sinusoidal wave is called a non-sinusoidal waveform. For example pulse square, symmetrical square triangular and saw-tooth are non- sinusoidal waves. When one quantity is dependent upon some other variable quantity varies with respect to others. In case of electronic circuits function usually means that current or voltage varies with respect to time. All these waveform are the function voltage or current with respect to time such as step, ramp and exponential are explained as under:

Step Function:

A step function shown in Fig. 1(a), makes an instantaneous jump from one steady value to another steady value. A step means an instantaneous change in level.

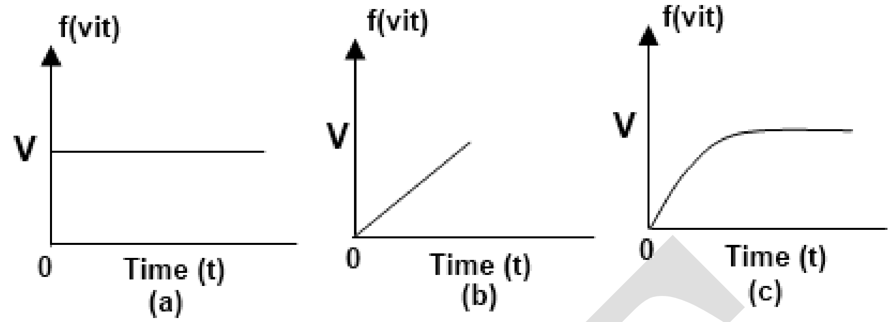


Figure 1 ***Functions***

In such a case, voltage maintains zero value for all times t < 0 and maintains the value V for all times t > 0 is called a step voltage.

Ramp Function:

A ramp function shown in Figure 1(b) isone that voltage increases or decreases linearly with time. Slope of the function is constant. In such a case, voltage is zero for t < 0 and increases linearly with time for t > 0.it is linear change in function with respect to time called a ramp.

Exponential Function:

An exponential function is a function of voltage that increases or decreases exponentially with time. In such a case, voltage is zero for t < 0 and increases nonlinearly with time t called an exponential voltage. The terms used for exponential are e^x and e^{-x}. Exponential quantity gap is known as an exponential curve.

Different Types of Waveforms

Let us now discus the pulse square, symmetrical square, Triangular and saw-tooth waveforms.

Pulse waveform

Figure 2(a) shows the waveform of an ideal pulse. The pulse amplitude is V and the pulse duration is t_p. It is evident from Fig. 2(b) and (c) that the pulse may be considered as the sum of the step voltage +V, whose discontinuity occur at t = 0 and a step voltage —V, whose discontinuity occurs at $t = t_p$. The pulse waveform find extensive use is almost every field of electronics such as communication, computer, defense equipment, etc.

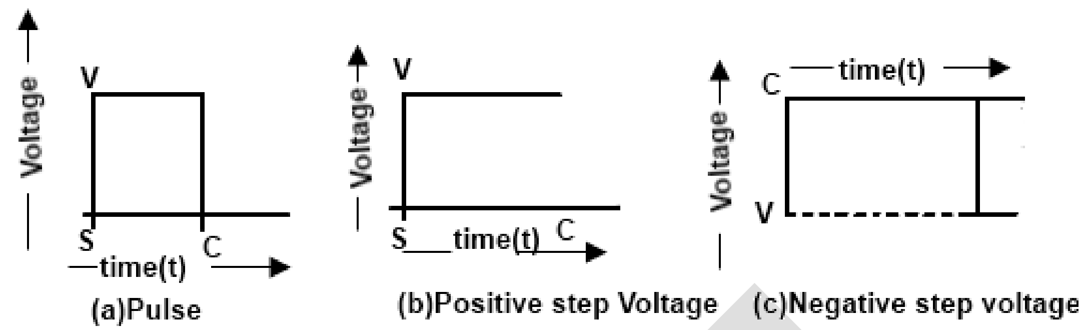


Figure 2

Square waveform

A waveform which maintains itself at one constant voltage level V_1 for a time T_1 and at another constant level V_2 for time T_2 and is repetitive with a period $T = T_1 + T_2$ as shown in Fig. 2 (a) is called a square waveform. The square waveform is used in digital electronic circuits, radars and as synchronizing pulses in television.

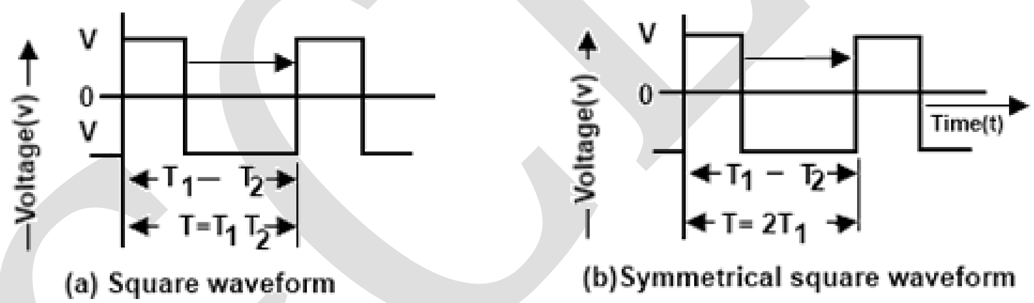


Figure 3

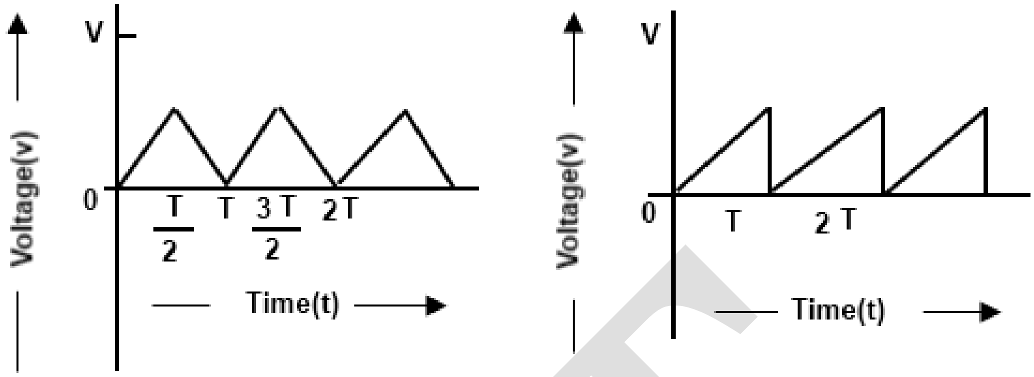
Symmetrical square waveform

A square waveform for which $T_1 = T_2 = T/2$ as shown in Fig. 3(b) is called a square waveform. It may be noted that because of the symmetry, the voltage levels V_1 and V_2 are equal and opposite $V_1 = —V_2$. The symmetrical square waveform is very useful in digital electronic circuits.

Ttriangular waveform

A waveform which increase linearly with time to a voltage level V for a time T/2 and then decreases linearly to its original level for a time T/2 and is repetitive with a period T as shown in Fig. 4(a) is called triangular waveform. It may be noted from this figure, that a triangular wave may be considered as the sum of ramp voltage, which increases at a rate of 2V/T for a time T/2 and the ramp voltage which decreases at a rate of —2V/T for the remaining time T/2. The triangular waveform is used in scanning circuits, where a uniform left-to-right scan is required as

In computer displays. These are also used in timing circuit for electronics applications.



(a) Trianglar waveform (b)Saw-tooth waveform

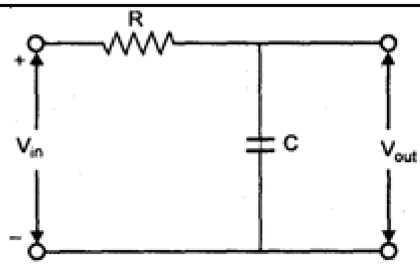
Figure 4

Saw tooth waveform

A waveform increases linearly with time to a voltage level V for a time T and then changes abruptly to its original level and is repetitive as shown in Fig. 4(b) is called saw tooth waveform. It is also called sweep waveform or time-base waveform. The saw tooth waveform is used in the scanning circuit of cathode ray oscilloscopes and televisions.

Differences between Low-pass and High-pass circuit showing circuit diagrams.

Low-Pass Circuit	High-Pass Circuits
(i) In a low pass circuit V_{out} is taken across the capacitor.	(i) In high pass RC data, the O/P voltage V_{out} is taken across the resistance.
(ii) It passes low frequency signals and blocks the high frequency signals.	(ii) It blocks P attenuates low frequencies, but allows high frequency signals to pass through it.
(iii)	(iii)



(iv) Current through the circuit is given as:

$$I = \frac{V_{in}}{R - j \times c}$$

(v) Output voltage is given as

$$V_{out} = \left[\frac{-j \times c}{R - j \times c}\right].V_{in}$$

(vi) Magnitude of amplitude is given by:

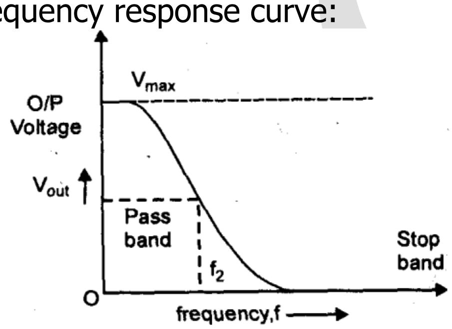
$$|A| = \frac{1}{\sqrt{1+\left(\frac{f}{f_2}\right)^2}}$$

Where f_2 = cut off frequency.

(vii) Phase angle:

$$\theta = \tan^{-1}\left(\frac{f}{f_2}\right)$$

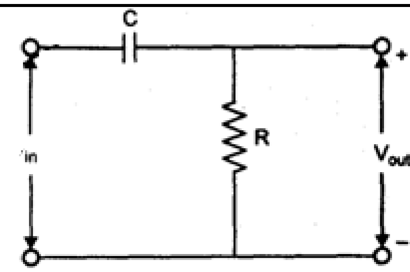
(viii) Frequency response curve:



(ix) At very high frequencies the capacitive reactance become very small so 0/p becomes equal to i/p.

(x) R-C circuits with time constant larger than time period of the input signal are used as by-pass capacitors.

(xi) It is used is generation of triangular and ramp waveforms.



(iv) Current through the circuit is given as:

$$I = \frac{V_{in}}{R - j \times c}$$

(v) Output voltage is given as:

$$V_{out} = \left[\frac{R}{R - j \times c}\right].V_{in}$$

(vi) Magnitude amplitude is given by:

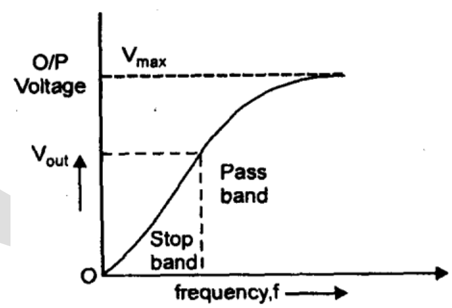
$$|A| = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}$$

where f_1 = frequency at which X_C = R.

(vii) Phase angle:

$$\theta = \tan^{-1}\left(\frac{f_1}{f}\right)$$

(viii) Frequency response curve:



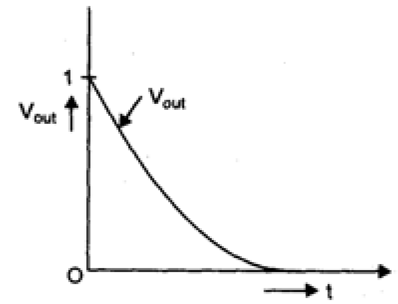
(ix) With the increase in frequency the reactance of the capacitor decreases and therefore, the output will be zero and gain increase.

(x) R-C circuits with RC >> T is employed in R-C coupling of amplifiers where distortion and differentiation of waveform is to be avoided.

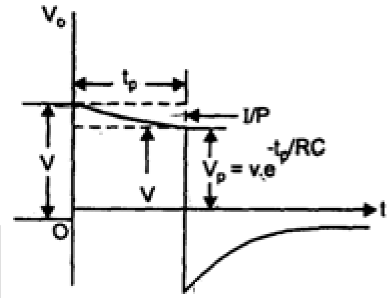
(xi) R-C circuits with RC << T is employed generate pipes for triggering electronic circuit such as flip-flop multivibrators.

Draw the standard waveforms used to obtain response of a R-C circuit diagrams.

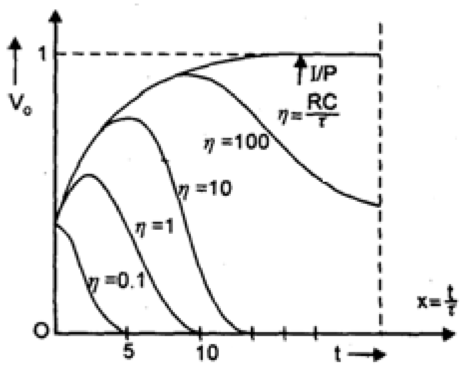
Ans. The standard waveforms used to obtain response of a RC circuit diagram are as under:



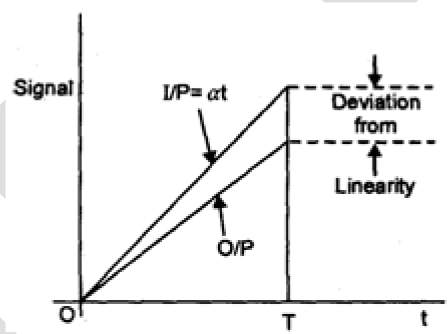
***Step voltage response of pass R-C circuit**



**** A step pulse after transmission through High-high:pass RC circuit**

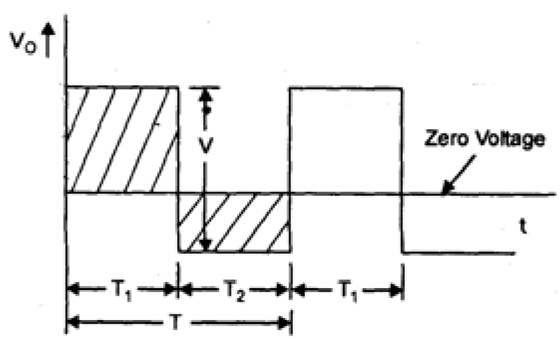


Response of a high-pass RC circuit to an exponential input.



Response of a high-pass RC circuit to a ramp voltage for

$\frac{RC}{\tau} >> 1.$



Output voltage for square wave input $\tau >> T$. Area A_1 = Area A_2.

In a low frequency series R-C circuit obtain unit step response if R = $1M\Omega$ and t (time constant) = 1 sec.

Ans. A step voltage v(t) is written as

$$v(t) = \begin{cases} 0 \text{ for } t < 0 \\ \text{V for } t \geq 0 \end{cases}$$

General solution for a single time constant circuit having initial and final values $v_0(0)$ and $v_0(\infty)$ Respectively is,

$$v_0(t) = v_0(\infty) + [v_0(0) - v_0(\infty)].e^{-t/\tau}$$

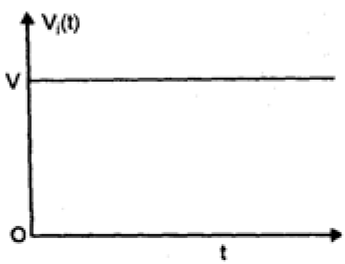
Substituting

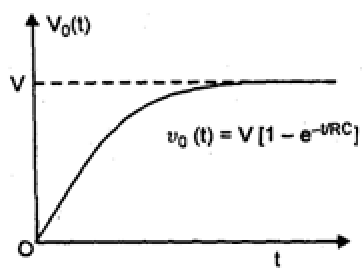
$$v_0(t) = \text{V}\left[1 - e^{-\frac{t}{\text{RC}}}\right]$$

If $\quad \text{V} = 1, \text{RC} = \tau = 1$

$$v_0(t) = 1.[1 - e^{-t/1}]$$

$$v_0(t) = (1 - e^{-t/1})$$





*The step waveform. **Output waveform of Rc low-Para filter

Note: This waveform is exponentially raising waveform as shown in fig. (b). this response reaches almost 'V' after a time't' greater than 5RC.

Define delay time, rise time, storage time and fall time in response Characteristics.

Ans. Time constant definition: The required for a capacitive circuit to reach its steady state or final voltage can be specified in terms of the constant denoted by τ The time constant in an RC circuit is τ = RC, while for an RL circuit is $\tau = \frac{\text{L}}{\text{R}}$

Time constant of a Raising exponential: Raising capacitor Voltage

$$v_0(t) = \text{V}\left[1 - e^{\frac{-t}{\text{RC}}}\right] \qquad ...(1)$$

Differentiating, $\frac{d\text{V}_c(t)}{dt} = \frac{\text{V}}{\text{RC}}.e^{-t/\text{RC}}, \left[\frac{d}{dt}.v_c(t)\right]_{t=0} = \frac{\text{V}}{\text{RC}}$

Time constant can be defined in terms of exponentially rising voltage as

(i) τ can be defined for a rising voltage as the time required for the voltage to reach its final value if the voltage continues to rise at its initial rate.
(ii) Sometimes, τ is defined as the time required for the voltage to increase to 63.2 percent of its final value.

Time constant of a Decaying Exponential

The decaying capacitor voltage

$$v_0(t) = V.e^{-t/RC} \quad ...(2)$$

By differentiating this equation initial slope of this decaying exponential as,

$$\frac{d}{dt}\left[V_c(t)\right] = -\frac{V}{RC}.e^{-t/RC}$$

$$\left[\frac{dV_c(t)}{dt}\right]_{t=0} = -\frac{V}{RC}$$

Taking the above decaying exponential voltage into account, time constant is defined in the following two ways:

(i) The time constant τ can be defined for an exponentially decaying voltage as the time required for the voltage to reach zero, if the voltage continues to decay at its initial rate.
(ii) Sometimes, the time constant τ is defined as the time required for the voltage to decay to 36.8 percent of its initial value.

Physical significance of time constant

The time constant 'τ' gives an indication of time needed for the circuit transient to disappear. After the disappearance of the transient state, the circuit reaches its steady state.
Theoretically a transient state persists for infinite time. However, we can always assume that the circuit has reached its steady state after a lapse of 5τ.
This implies that a circuit with a small 'r' ensures fast response that is, it reaches its steady state in a short-time.
Similarly, if the 'r' of a circuit is large that circuit takes long time to attain, its steady state.

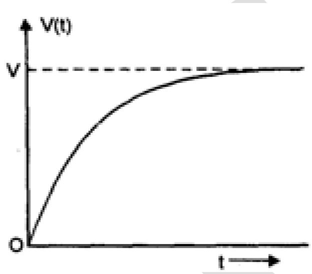


Fig. (a) Raising exponential waveform

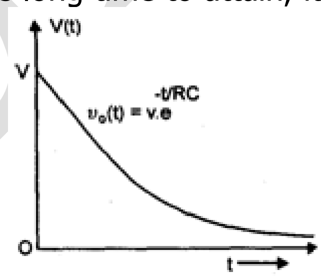


Fig. (b) Decaying exponential waveform

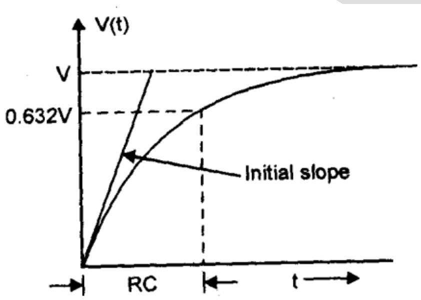


Fig. (c) Time constant of raising exponential waveform

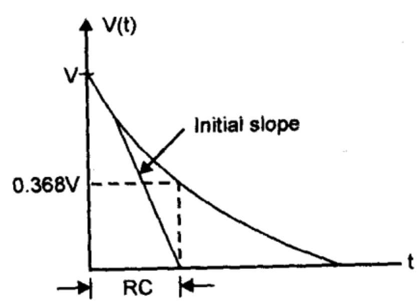
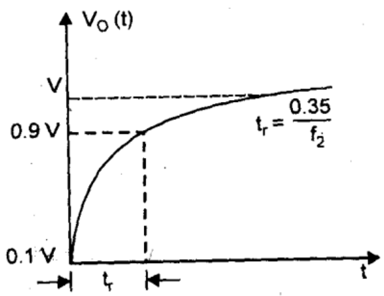


Fig. (d) Time constant of decaying exponential waveform

Rise time: The rise time of the step response is defind as the time taken for the exponentially raising output waveform to rise from 10% to 90% of its final value 'v'.



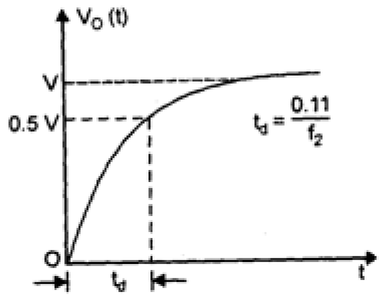


Fig. (a) Definition of Rise time **Fig. (b) Definition of Delay time.**

The definition of rise time is graphically indicated in fig. (a). Let t_1 and t_2 are the times at which the waveform reaches 10% and 90% of its final value V_1 respectively,

$$0.1\ V = V[1 - e^{-t_1/RC}]$$

$$0.9\ V = V[1 - e^{-t_2/RC}]$$

From this, we can determine the values of 't_1' and 't_2'

$$t_1 = 0.1\ RC \qquad ...(1)$$

$$t_2 = 2.3\ RC \qquad ...(2)$$

$$t_r = t_2 - t_1 = 2.2\ RC$$

$$f_2 = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi f_2}$$

$$t_r = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} \qquad ...(3)$$

Expression for delay time: The delay time t_d is defind as the time taken for the exponentially raising output waveform to rise from Zero to 50 percent of its final value 'v'.

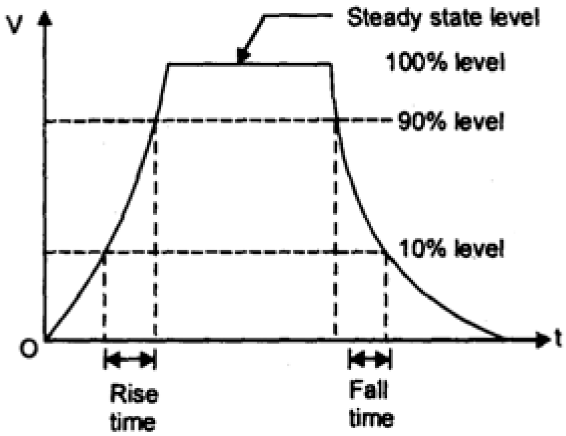
$$0.5V = V\left[1 - e^{-\frac{td}{RC}}\right]$$

$$t_d = 0.7RC = \frac{0.7}{2\pi f_2} = \frac{0.11}{f_2}$$

$$t_d = \frac{0.11}{f_2} \qquad ...(2)$$

Storage time: It is the time when the output waveform becomes constant or reaches the steady state.

Fall time: The time pulse takes to decreases from 90% to 10% of its normal amplitude is called fall time.



Q.5. If RC time constant of a high pass filter is made increasingly smaller in comparison of duration of input waveform. Is the width of the output pulse increased or decreased. Explain your answer.

Ans. Pulse input: The response to a pulse for times less than the pulse t_p width is the same as that for a step input and is given by

$$v_0(t) = V.\left[1 - e^{\frac{-t}{RC}}\right] \qquad ...(2)$$

At the end of the pulse, the voltage is V_p and the output must decrease to zero from this value with a time constant RC as indicated in Fig. (a). Note the waveform distortion that has resulted from passing a pulse through a low-pass RC circuit. In particular it should be observed that the output will always extend beyond the pulse width t_p, because whatever charge has accumulated on the capacitor 'C' during the pulse cannot leak off instantaneously.

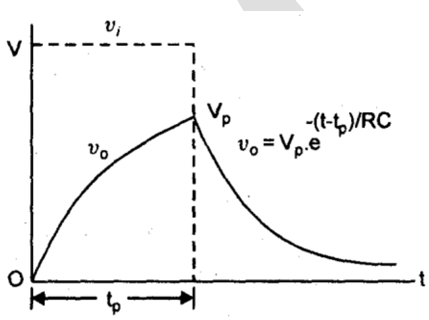


Fig. Pulse response of the Low-pass RC circuit.

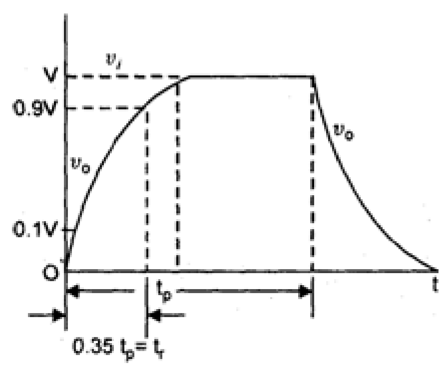


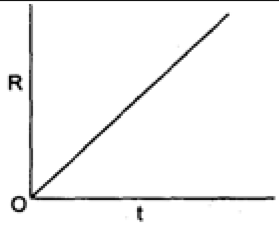
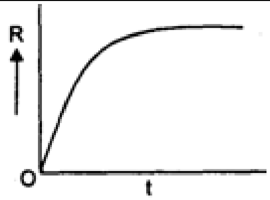
Fig. Pulse response for the case $f_2 = \left(\frac{1}{t_p}\right)$

If it is desired to minimise the distortion then the rise time must be small compared with the pulse width. f_2 Is chosen equal to $\left(\frac{1}{t_p}\right)$, then, $t_r = 0.35\ t_p$.
The 0/P is as pictured in fig. (b), which for many applications in a reasonable reproduction- of the input.
We often use the rule of thumb that a pulse shape will be preserved if the 3,-dB Frequency is approximately equal to the reciprocal of the pulse width. Thus to pass a 0.5 μsec reasonably well requires a circuit with an upper 3-dB frequency of the order of 2MHz.

For a high pass RC circuit, $f_1 = \frac{1}{2\pi RC}$. if RC is smaller, f_1 will increase. So pulse width is inversely proportional to frequency.
Pulse width of the output will decrease.

Difference between linear and non-linear wave shaping circuits.

Linear Wave Shaping	Non-Linear Wave Shaping
(i) It involves passage of signal through linear system.	(i) It involves passage of signal through non-linear systems.
(ii) The operation involved are linear operations such as integration, differentiation, summation, filtering etc.	(ii) It permits transformation of analog signal to digital signal and vice-versa.
(iii) Some of the important on-sinusoidal waveform are the step, pulse, square, wave, ramp and exponential waveform.	(iii) Eg. (1) Clipping operation; and (2) rejection of negative spikes by rectification are non-linear operation.
(iv) Typical example is low-pass and high-pass R-C circuit.	(iv) Clamping circuits. Example is an integrator using an OP-AMP.
(v) It includes R-C circuit R-L and R-L-C circuit.	(v) It includes diode, zener diode, transistor, vacuum tube, etc.
(vi) It can be described by linear differential wave equations.	(vi) When any wave form is applied at the input of non-linear circuit.

linear wave shaping and give examples.

Wave-shaping may be defined as the process of generating new waveforms from older waveforms by employing certain physical systems.
Linear wave shaping involves passage of signal through linear systems such as R-C , R-L and R-L-C circuits and the operations involved are linear such as integration , differentiation summation , filtering etc. example of linear wave shaping.
(i) High- pass and low- pass R-C circuit.
(ii) R-C differentiator.
(iii) R-C intergrator.
(iv) R-L circuits.
(v) R-L-C circuits.
(vi) Attenuators.
In pulse circuitry, there are number of non-sinusoidal waveform which appears regularly. The most important of them are : step, pulse, square wave, Ramp and exponential waveforms.

Attenuators

Compensated Attenuators	Uncompensated Attenuators
Compensated attenuators are those circuits which are use to reduce the rise time due to stray capacitance by introducing capacitors to balance the stray capacitance.	Normally the output of the attenuator is fed to a circuit that offers a reactive load. This reactive load is generally the stray input capacitance of an amplifier. When we consider the stray capacitance, the purely resistive attenuator becomes an uncompensated attenuator.

Perfect Attenuators : In most of the electronic applications, the amplitude of the signal is magnified with the help of an amplifier. There are also instances, where the signal amplitude has to be reduced without affecting the signal waveshape. Attenuator is a circuit that reduces the amplitude of the signal without leading to any distortion in the signal waveform. The CR0 probe can be cited as one such example. The high-pass filter and low-pass filter circuits, reduce the amplitude or attenuate the input signal.
In uncompensated attenuators, the stray capacitance makes attenuation frequency dependent.

The circuit in fig. 2(b) can be redrawn as a low-pass filter circuit by applying Thevenin's theorem. Here, R becomes the parallel combination of 'R_1' and 'R_2'.
Since it is not possible to remove this stray capacitance, one can neutralise the presence of the stray capacitance. This is done by compensating the attenuator by connecting 'C_1' across 'R_1'.
The condition for a circuit to be precisely satisfied for perfect compensation is,

$$R_1C_1 = R_2C_2.$$

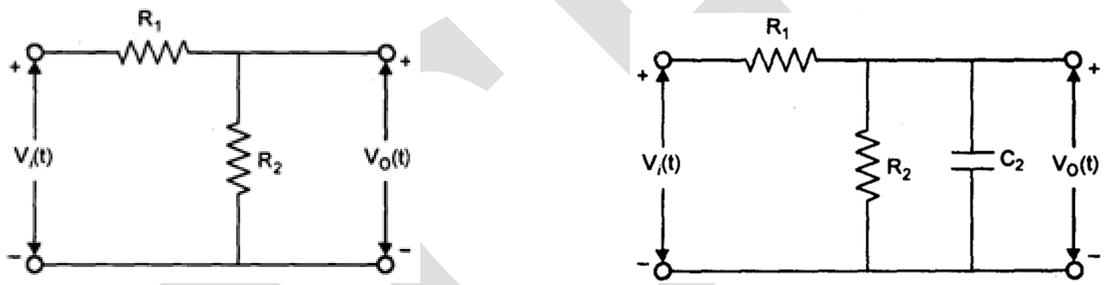
This can be satisfied by redrawing the circuit in Fig 2(c) as a bridge circuit shown in Fig. 2(d). The current in the short circuit branch A-B becomes zero when the bridge is balanced. When no current flows through this branch, the output voltage can be again written as,

$$v_0(t) = \frac{R_2}{R_1 + R_2}.v_i(t)$$

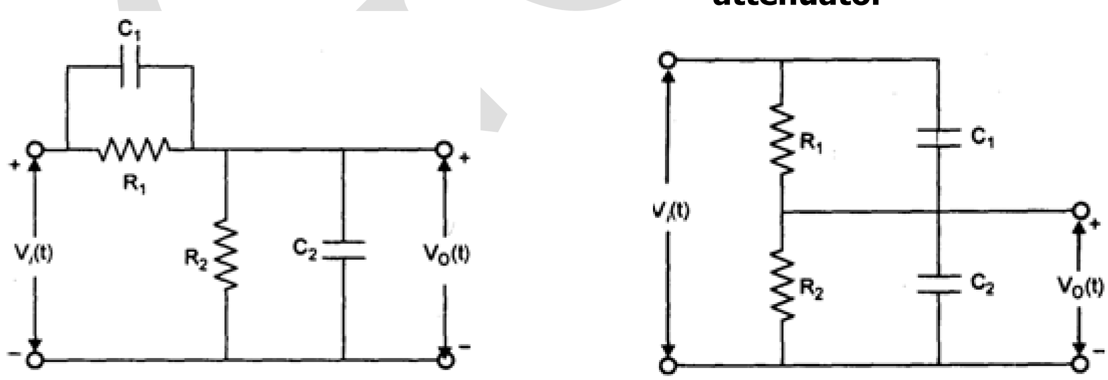
$$R_i \times \frac{1}{2\pi f C_2} = R_2 \times \frac{1}{2\pi f C_1}$$

$$\boxed{C_1 = \frac{R_2C_2}{R_1}}$$

This is the condition for perfect compensation. However, it is difficult to satisfy this condition exactly in a practical situation.



(a) The perfect Compensator **(b) The uncompensated attenuator**



(c) The compensated attenuator **(d) The compensated attenuator redrawn as a bridge**

Fig. 2 The compensated attenuator.

Problems:

What is the expression of time constant (τ) for an R-C circuit with R = 500 Ω and C = 20 μF ? Show that the unit of τ is second.

Ans. We have

Resistance R = 500 Ω and C=20 μF

Time constant of an R-C circuit is given as

$$\tau = RC = 500 \times 20 \times 10^{-6} = 10{,}000 \times 10^{-6} = 10^{-2} \text{ sec}$$
$$= 0.01 \text{ seconds}$$

For a simple circuit

$$R = \frac{V}{I}, \text{ and } C = \frac{1}{V}\int i\,dt$$

$$\tau, \text{ the time constant} = RC = \frac{V}{I} \times \frac{1}{V}\int i\,dt = \frac{1}{I}\int i\,dt$$

Taking the units = $\frac{\text{Ampere — sec Ampere}}{\text{Ampere}}$

- Unit of 'τ' is seconds.

or

Dimensions of R and C are $[mL^2.T^{-3}.I^{-2}]$and$[m^{-1}L^{-2}.T^4.I^2]$

- $T = [mL^2.T^{-3}.I^{-2}].[m^{-1}L^{-2}.T^4.I^2] = [T]$
- Unit of 'r' is second.

Ringing Circuit

Ans. Ringing circuits are those which generate asequence of pulses spaced regularly intime these circuits have undamped oxillations depending on the number of ringing duty cycles recuired Consider the ringing circuit of Fig. A.1. in which there is an initial voltage $\overline{V_0}$ across the capacitor 'C' as well as an initial inductor current I. It is now convenient to introduce a parameter Δ, defined as the ratio of coil current to resistor current at t = 0.

$$\Delta = \frac{I}{V_0/R} = \frac{IR}{V_0} \quad ...(A.1)$$

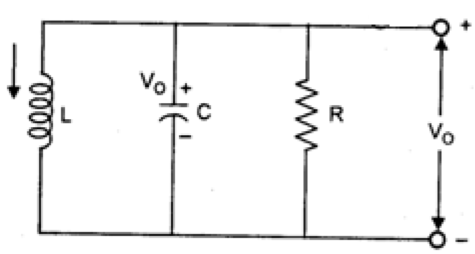


Fig. A. 1 Ringing circuit with initial current 'I' in inductor and initial voltage V_0 across capacitor.

The output $\frac{v_0(t)}{V_0}$ can be expressed as a function of a time $\left(x = \frac{t}{T_0}\right)$ with Δ and 'k' as a parameters the definations of 'k' and T_0' are

$$k = \frac{1}{2R}\sqrt{\frac{L}{C}} \text{ and } T_0 = 2\pi\sqrt{LC} \quad ...(A.2)$$

Critical Damping, k=1

$$\frac{v_0(t)}{v_0} \quad [1-(1+2\Delta)(2\pi x)]\,.\varepsilon^{-2\pi x} \quad ...(A.3)$$

Overdamped with $4k^2 >> 1$,

$$\frac{v_0(t)}{V_0} = -\left[\frac{1}{4k^2} + \Delta\right] \varepsilon^{-\pi x/k} + (1+\Delta)\ \varepsilon^{-4\pi kx} \quad ...(A.4)$$

Underdamped, k <1

$$\frac{v_0(t)}{V_0}\left[-(1+2\Delta)\,.\frac{k}{\sqrt{1-k^2}}\,.\sin 2\pi\sqrt{1-k^2x} + \cos 2\pi\sqrt{1-k^2x}\right].\varepsilon^{-2\pi kx} \quad ...(A.5)$$

These responses are plotted in Figs. A.2, A.3 and A.4.

We note that even for the critically damped case, there may be an undershoot i.e., the output which starts at a positive value drops to a negative value before returning asymtotically to zero.

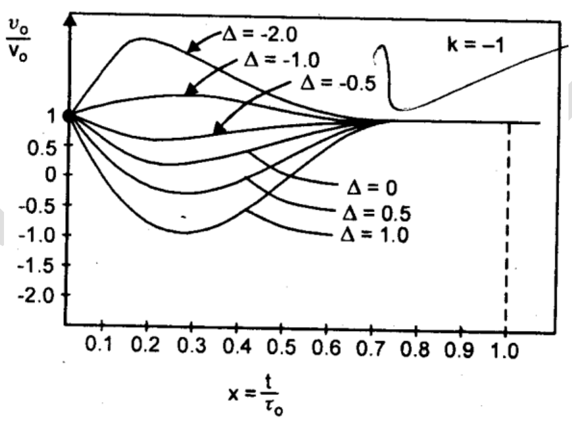


Fig. A.2. of equation (A.3).

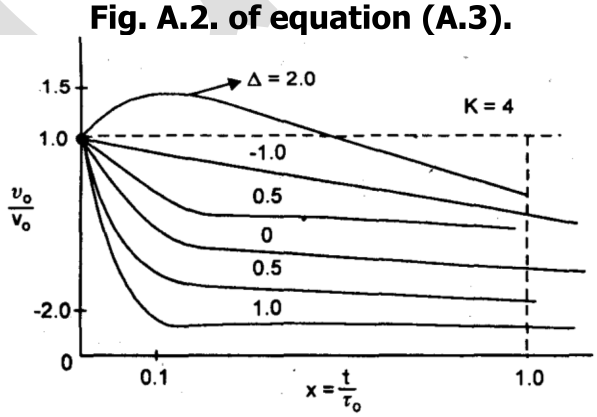


Fig. A. 3. (Plot of eq. (A.4) with k = 4.

If V_0 ad I have the relative polarities indicated in Fig. A. 1 then Δ is positive. If the relative polarities differ from those indicated, the 'Δ' is negative. For a negative A, the output may rise first (see the curve for 'Δ' = —2.0) ; before falling to zero. The physical reason for this initial increase in output is that the inductor current (with the polarity opposite to that in Fig. A.1.) may charge the capacitor to a more positive voltage before 'C' discharges through the resistor.

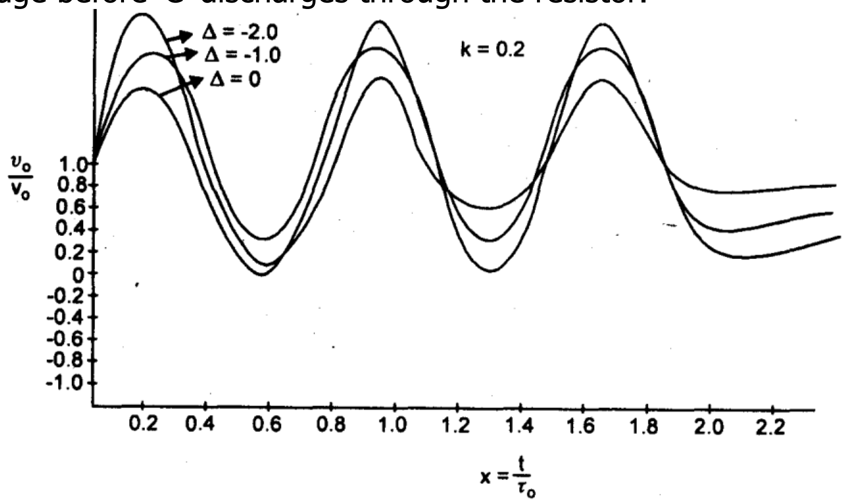


Fig. (A.4) Plot of equation (4.5) with k = 0.2.

We see that the waveform depends upon the inductor and resistor currents (the sign and magnitude of Δ) and upon the amount of the damping (the value of k).

The areas under each curve of Fig. A.3, Fig. A.2 and Fig A. 4. is $\left(\frac{-k.\Delta}{\pi}\right)$. This canbe verified by direct integration or much more easily by proceeding as follows:

Since $v_0(t) = \alpha.\frac{di}{dt}(t)$

Or $\frac{v_0(t)}{V_0} = \frac{L}{V_0.T_0}.\frac{di}{dx}(t)$

Then Area $= \int_0^\infty \frac{v_0(t)}{V_0}dx = \frac{L}{V_0.T_0}\int_0^\infty di(t)$

$= \frac{-LI}{V_0.T_0} \times \frac{-L.\Delta}{R.T_0}$

Area $= \frac{-L.\Delta}{\left(\frac{1}{2}K\right):\sqrt{L/C}} \times \frac{1}{2\pi\sqrt{LC}}$

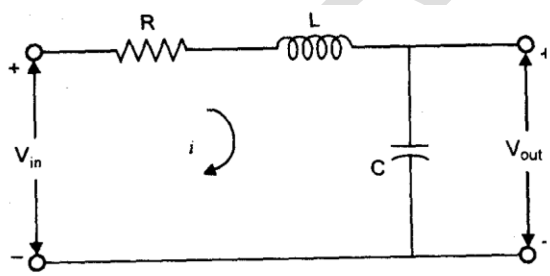
$$= \frac{-K\Delta}{\pi} \qquad ...(A.6)$$

User : These circuits are employed in timing circuit in automatic control circuit.

Why RC circuit is preferred over RL circuit in wave shaping?

Ans. Practically, RL circuit is rarely used if a large time constant is required. This is because the time constant of RL circuit is = $\left(\frac{L}{R}\right)$ and to get large time consnntant 'L' should be large. This is possible only with iron core inductor which is very large, heavy and expensive compared to capacitor for a similar application. Such an inductor is shunted with a large amount of stray capacitance. The iron properties are also non linear. These things cause distortions which is not desirable.
Thus, RL circuit is used only if small time constant is required. For such a case, small and in expensive air core inductor is used.

The transient response of a series RLC circuit with step input.



$$i(t) = iR + L\frac{di}{dt} + \frac{1}{C}\int idt$$

$$I(s) = \frac{1}{L} \times \left[\frac{1}{s^2 + \frac{R}{L}s + \frac{1}{LC}}\right]$$

$$s_1, s_2 = \frac{-R}{2L} \mp \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Case I: When $\left(\frac{R}{2L}\right)^2 > \frac{1}{LC}$;

i.e. R > $2.\sqrt{\frac{L}{C}}$, Roots are real and different.
Circuit is over-damped.
No oscillation in the output.

Case II: When R = $2.\sqrt{\frac{L}{C}}$;

both roots are real and equal.

$$S_1 = S_2 = \frac{-R}{2L}$$

$$i(t) = \frac{1}{L}\left[t.e^{-\frac{R}{2L}.t}\right]$$

Circuit is critically damped.

Case III : When $R < 2.\sqrt{\frac{L}{C}}$,

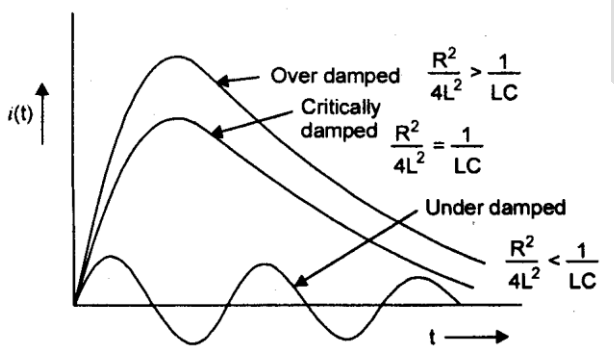
Roots are complex and conjugate of each other.

Circuit is under-damped and output will have oscillations.

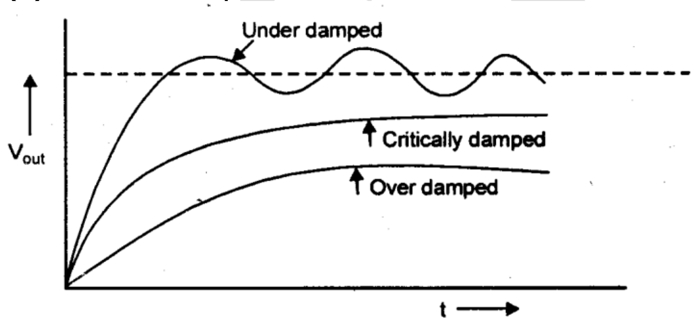
$$S_1, S_2 = \frac{-R}{2L} \mp 2j\omega_0$$

And

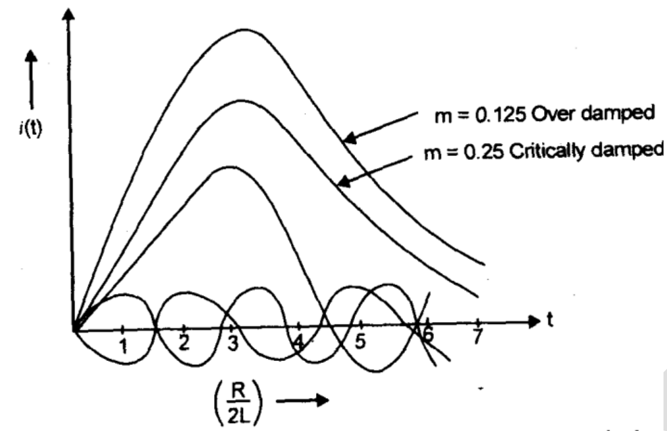
$$i\ (t) = \frac{1}{w_0 L}.e^{\left(-\frac{R}{2L}.t\right)} \sin w_0 t$$



(a) Current Respons



(b)Voltage Response



(c)Transient Response of senes RLC ckt. when step input is applied

UNIT-5

UNIT-5
Switching characteristics of Devices:

Enumerate at least three applications of transistors.

At least three applications of transistors are:

(1) Digital logical circuit
(2) Switching applications
(3) Amplifier
(4) Clipper
(5) IC`s

What is the use of commutating capacitor in transistor?

The transistor is expected to make a transition from saturation to cut- off on the falling edge of the input pulse. There is going to be a delay in this transition since the transistor can enter cut – off only when all the stored charge in its base is removed.

Let us analyze this circuit with a variable capacitor 'C' connected across the series resistance 'R. We know that capacitor behaves like a short circuit for sudden changes in voltage.

On the falling edge of the input voltage 'C' functions as a short-circuit. However, capacitor 'C' attempts to charge towards the pulse amplitude 'V' if it is given the required time and when it is fully charged to 'V" it behaves .as an open circuit.

The collector waveform [Fig. I. (b)] is observed for the purpose of estimating the value of variable capacitor 'C' shown in Fig. 1(a). When the transistor enters cut-off, after a delay all the accumulated charged T in the base is transferred on the capacitor 'C' It is clear now that the capacitor 'C' is fully charged to 'V' and holds the total charge Q_T, which can be expressed as,

$$Q_T = CV \qquad \dots (1)$$

The shape of the output waveform for different values of 'C' is shown in Fig. 1(b). If we choose a large value of 'C', the stored charge Q_T is certainly transferred on to it. In this case, the output waveform commences with a large initial slope and its rate of change slows down as it reaches its final value V_{CC}.

If we make the value of 'C' smaller, we find the output waveform reaching its final value V_{CC} commencing with a small initial slope.

The two extremes of the capacitor 'C' are 'C' =0 and C = $\left(\frac{Q_T}{V}\right)$

A practically suitable value of 'C' can be obtained experimentally with rise time [Fig. 1(b)] of the output waveform as the guideline. This diagram clearly shows the effect of 'C' on the rise time of the collector voltage waveform. The principle for dividing the value of 'C' is to ensure that the output waveform rises to its final value more rapidly than the decaying rate of the stored charge of the base.

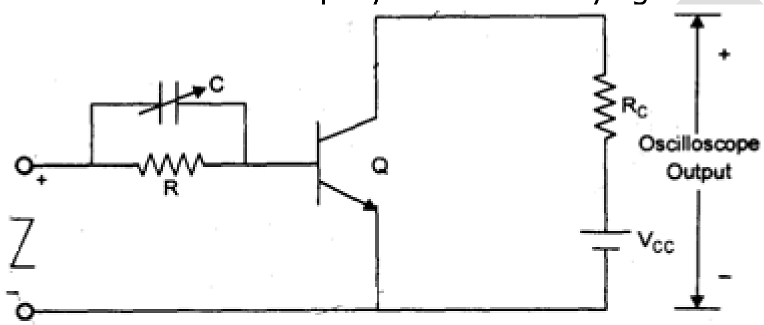


Fig.1. (a) Commutative capacitance in a CE transistor switch

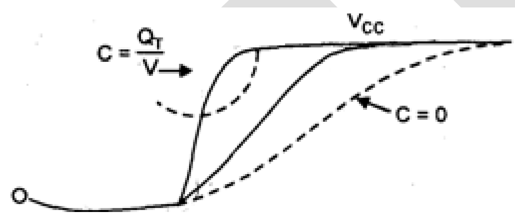


Fig.1. (b) Effect of commutative capacitance on t e output waveform

It is not possible to have an exact value. Q_T as it depends on several factors like the operating point power supply voltage V_{CC} and temperature. The capacitor 'C' can be called as a speed – up capacitor as it associated with speedy removal of stored charge from the base. The value of Q_T supply by the manufacture is adequate for the theoretical calculation of 'C' making use of equation (1). The value of 'C' can be adjusted to suit a given application by employing experimental approach discussed above.

This experimental approach would result in the correct estimation of 'C' only when the rise time of the input pulse is small compared to time constant associated with the exponential decay of the stored charge.

If this precaution is not taken, there.Is a possibility for a small portion of the stored charge to escape from the base due to recombinations during the transition interval.

Under these conditions, the value of Q_T computed using equation 1 would be less than its actual value. The speed up capacitor is also known as the commutative capacitor, as it plays an important role in the change of stable states of a bistable multivibrator.

What is an ideal diode? How does an actual diode differ from an ideal diode?

Ans. Ideal diode: It is two terminal device and permits only unidirectional conduct. It conducts well in the forward direction poorly in reverse direction. It would have ideal if it acted as a conductor with zero resistance or zero voltage drop across it, when reverse bised. The volt ampere characteristics of such an ideal diode have been as shown in Fig.1 (b). An ideal diode acts like an automatic switch. The switch is closed when diode is forward biased and is opened when reverse baised.

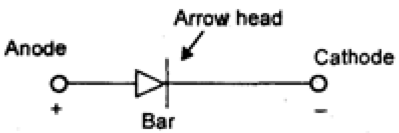


Fig. 1 :(a) Ideal diode

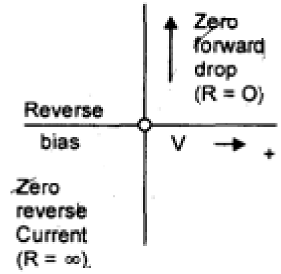


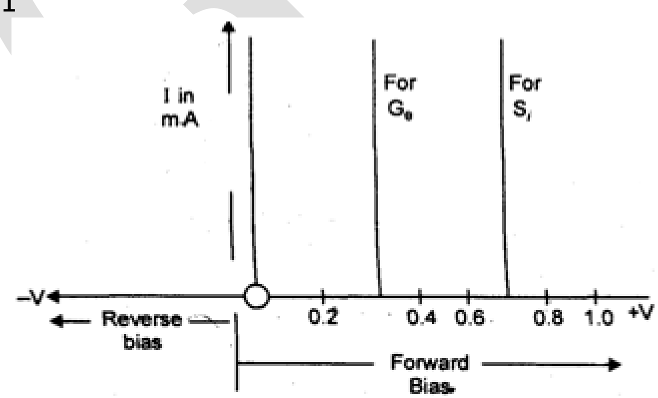
Fig. 1(b) ideal diode Characteristics

IN Forward Bias **In Reverse bias**

Fig. 1. (c) Switch Analogy

Ideal diode is different from actual diode because, no diode can act as ideal diode. An actual diode does not behave as a perfect conductor when forward biased and as perfect insulator when reverse biased. Neither it offers zero resistance when forward biased nor infinite resistance when reverse biased.

However, there are many applications in which diodes can be assumed to be nearly ideal devices, if the voltage drop across the diode when it is forward biased i.e. v is taken into account. In cases when the circuit supply voltage V is much larger than the forward voltage drop v, v can be assumed constant without introducing any serious error. Also, the diode forward current 'I' is usually so much larger than the reverse saturation current I_0 so that the I_0 can just be ignored.Thease e assumptions lead to a nearly ideal or approximate characteristics for germanium silicon diodes as illustrated in fig. 1



Explain various transistor switching times.

Ans.1. The time interval between the instant of application input pulse and output (collector) currant to attain 10 percent of its maximum value is termed as the delay time t_d .

2. Rise time, t_r is defined as the time required for the output currant I_C to go from 10% to 90% of its maximum value.

3. The sum of delay time, t_d and rise time, t_r is called the turn-ON time, t_{ON}.

i.e. $t_{ON} = t_d + t_r$

4. TURN- OFF time t_{OFF} is made up of a storage time, t_s and a fall time t_F.

i.e. $t_{OFF} = t_s + t_F$

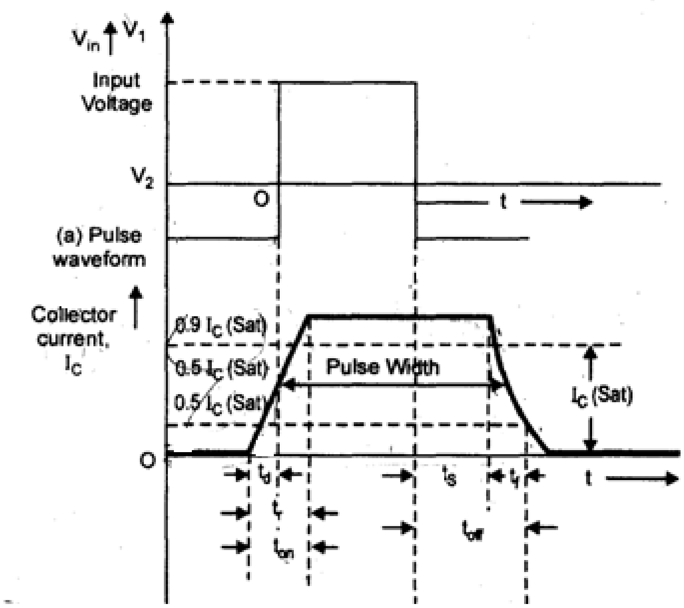
5. Storage time, t_s is defined as the time interval between the end of the input pulse (trailing edge) and when the collector current falls to 90% of its maximum value.

OR

Storage time, t_s is equal to the sum of time taken in removing excess charge stored and the time taken by collector transition capacitance to discharge to 90% of its maximum but major portion of the time is taken in removing excess charge storage.

The time duration of the output pulse measured between two 50% levels of rising and falling waveform is known as the **pulse width**.

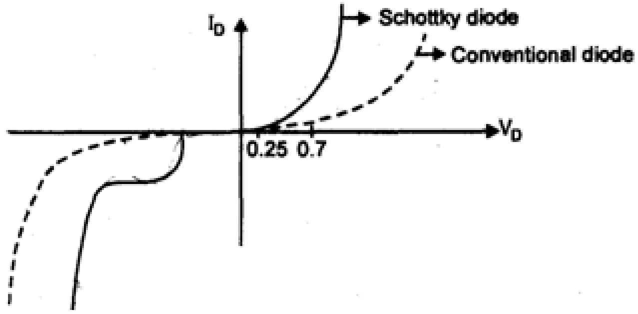
For a fast-switching transistor, turn-on time t_{ON} and turn-off time t_{OFF} must be of the order of nano seconds.



Fall time: The time required for the collector to drop from 90% to 10% of the saturation current is defined as a fall time t_F.

Why is storage time eliminated in Schottky transistor?

Ans.



The reverse recovery time is so short in small signal diodes that its effect cannot be noticed at frequencies below 10MHz or so. It is very important well above 10MHz.

Schottky diode has no depletion layer eliminating the stored charges at the junction. Because of lack storage charge schottky diode switch off faster then an ordinary diode. Infect, schottky diode easily rectify frequency exceeding 300Mz.

How does the commutating capacitor reduces the transition time of a transistor.

The transition capacitance plays an important role in switching circuits using diodes.

Mostly, t_{rr} few nanoseconds to one micro second in most commercially available switching diodes.

They are specially manufactured having t_{rr} as small as few Pico second.

The total switching time t_{rr} puts the limit on the maximum operating frequency of the diode. Hence, is an important data sheet specification.

To minimise the effect of the reverse current, the time period of the operating frequency must be at least ten times t_{rr} .

$$T = 10\, t_{rr}$$

$$f_{\max} = \frac{1}{T} = \frac{1}{10 t_{rr}}$$

Where $f_{\max}$ is the maximum operating frequency.

How is a transistor used as a switch.

Ans. A transistor can be employed as an electronic switch. Operating a transistor as a switch means it at either saturation or cut-off nowhere else along the load line. When a transistor is saturated it is like a closed switch from collector to emitter. When a transistor is cut off it is like an open switch.

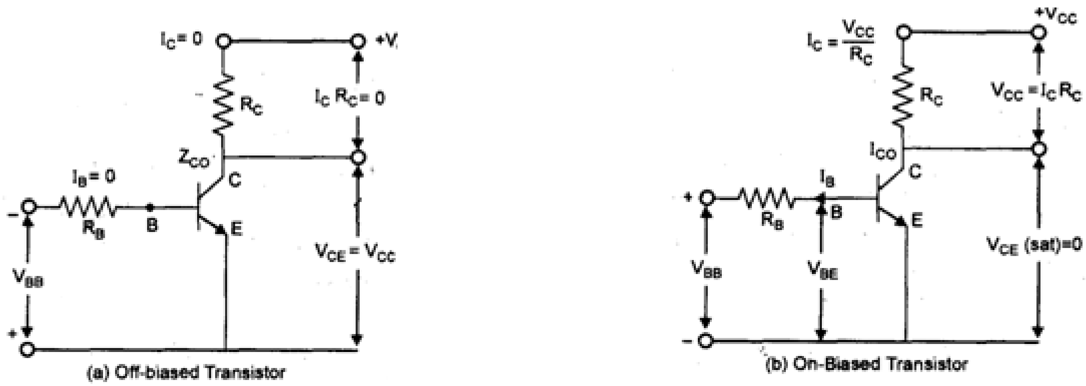
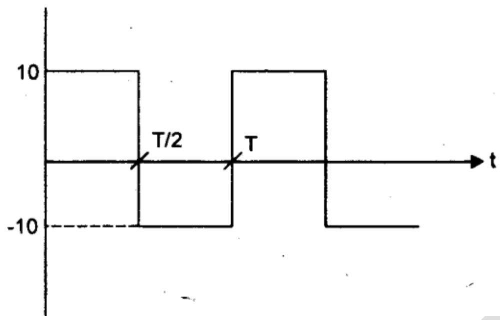
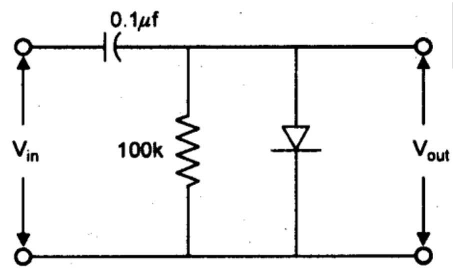


Fig. Operation of a Transistor as a switch

Giving proper justification, draw the output voltage waveform across diode (assume deal) for input waveform shown below:





Ans. When the input is -1OV, the diode is reverse biased.

Reactance of capacitor at 1 KHz= $\left(\frac{1}{2\pi f C}\right)$

$$= \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}} = 1592\Omega.$$

Current at (—10V) = $\frac{-10}{1592}$ = -6.28 Ma

Output voltage V_{out} = Voltage across diode

= Voltage across resistor lOOkΩ

= —6.28 x 10^{-3} x 100 x10^3

= -6.28 x 100

= - 628 Volt.

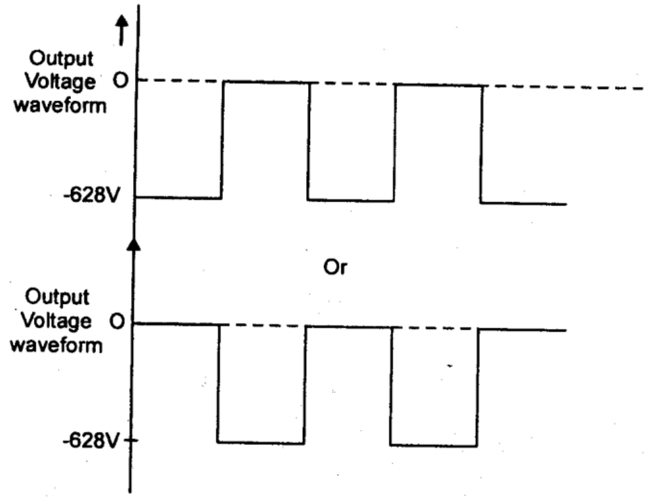
When the input v_{in} goes to +5V, the capacitor can't charge as its time constant is very large as compared to duration of pulse.

RC =100x10^3x0.lxlO_6

= 0.1 X 10^{-1} = 0.01 sec = 10 m sec.

Pulse width of the input = $\frac{T}{2} = \frac{1}{2f} = \frac{1}{2000}$ =0.5msec.

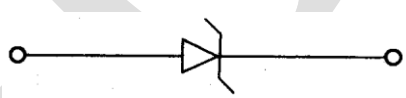
The diode can't conduct as it is an ideal diode



Uses of Schottky diode.

Schottky diode: At low frequencies the conversiol diodecan easly turn off by changing its bias from forward to reverse.But at very high frequencies the conversiol diode shows a tendency to store charge and there is noticiable current in reverse half cycle. During forward biased , it is not possibale for all the carrier in deplition region to recombine. Some carriers exist in deplition region which are not recombined.Now if the diode is suddenly reverse biased, the carriers exist in deplition region can flow in reverse direction for some time. But for large life time of these carrier, longer is the flow of current in reverse half cycle. Hence, there is the limitation on the frequency range for which conventional diode can be used.

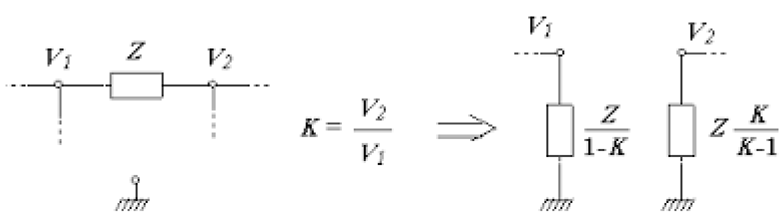
The diodes which manufactured to solve this problem of fast switching are called schottky diode



15.Additional/missing topics

1. Millers theorem

The Miller's theorem establishes that in a linear circuit, if there exists a branch with impedance Z, connecting two nodes with nodal voltages V_1 and V_2, we can replace this branch by two branches connecting the corresponding nodes to ground by impedances respectively $Z / (1-K)$ and $KZ / (K-1)$, where $K = V_2 / V_1$.



2. Positive feedback amplifiers

Positive feedback is a process that occurs in a feedback loop in which the effects of a small disturbance on a system include an increase in the magnitude of the perturbation.[1] That is, *A produces more of B which in turn produces more of A*.[2] In contrast, a system in which the results of a change act to reduce or counteract it has negative feedback.[1][3]

Mathematically, positive feedback is defined as a positive loop gain around a closed loop of cause and effect.[1][3] That is, positive feedback is in phase with the input, in the sense that it adds to make the input larger.[4][5] Positive feedback tends to cause system instability. When the loop gain is positive and above 1, there will typically be exponential growth, increasing oscillations or divergences from equilibrium.[3] System parameters will typically accelerate towards extreme values, which may damage or destroy the system, or may end with the system latched into a new stable state. Positive feedback may be controlled by signals in the system being filtered, damped, or limited, or it can be cancelled or reduced by adding negative feedback.

RC oscillators employ resistors and capacitors and are used to generate low or audio-frequency signals. Hence they are also known as audio-frequency (A.F) oscillators. The tuned or LC oscillators are not suitable at low-frequencies because the size of inductors and capacitors becomes very large. In these oscillators the single stage of the amplifier amplifies the input signal and produces a phase shift of 180°. To obtain positive feedback for sustained oscillation, the output of first stage is fed to a phase shift network to produce an additional phase shift of 180°. Thus a total of 360° phase shift which is equivalent to zero occurs. This principle is used in phase shift-oscillators. The most important types of RC feedback oscillators are phase shift and wein bridge oscillators.

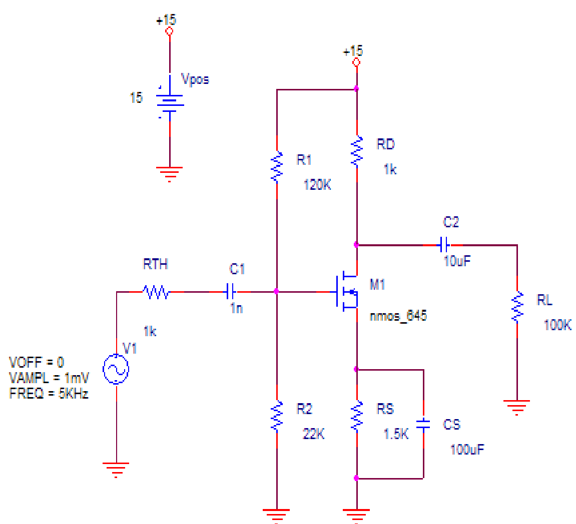
3.MOSFET Frequency response

he frequency response of a **BJT** or **MOSFET** can be found using nearly the exact same process, with the only variations being caused by a single resistor and simple naming conventions that differ between the two devices.

Before we start let's think a little bit about what we're doing:
Our goal is going to be to find the pole(s) of the circuit.
Okay? What is a pole and why do I care where it is?
A pole is a frequency at which the gain of the device rolls off. (remember that when it rolls off , it will be at the -3dB frequency with a slope of -20dB/decade)

We care because if the gain of a device rolls off at a certain frequency, then we won't be able to amplify a signal above that frequency very well because the gain will be decreasing by 20dB/decade.

The procedure is nearly identical whether we are using a BJT of a MOSFET, but we will work each of them side by side just in case there might be any confusion, and we'll follow these steps as we go through. (we will also use some values that came from the output file when running a simulation of this circuit in Cadence (or PSPICE)



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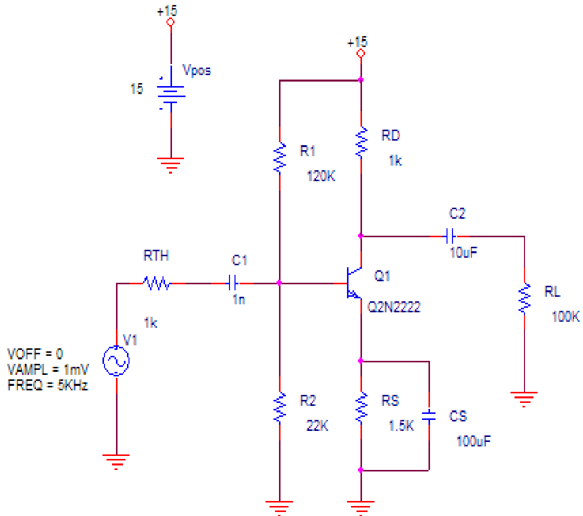


1. Take a look at one of the circuits and see what you notice, how about the MOSFET. This step is just to help us with our knowledge understanding of the circuit.

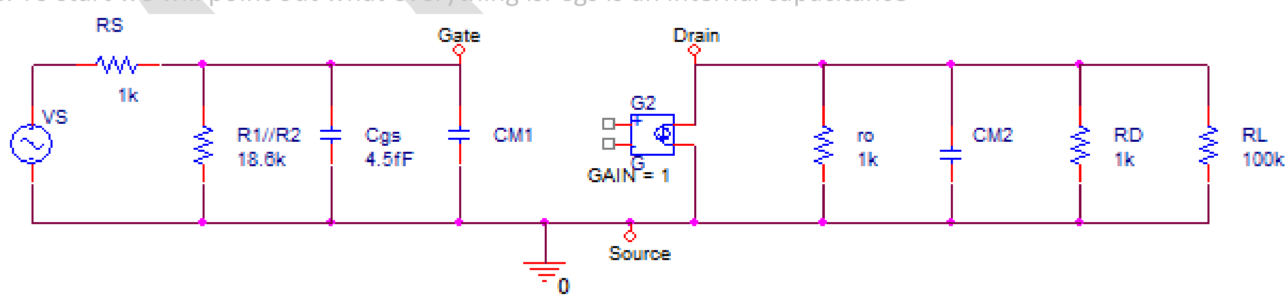
- At a glance it just looks just like another MOSFET right? Sure is, but let's take a look at a few things just for kicks. Notice that it is using a bypass capacitor at the source so we don't have to worry about R_s(at when working with high frequency). Since the capacitor $C_s$bypasses $R_s$to ground, you should notice that this is a common-source amplifier. You could notice the Values for $R_1$and $R_2$and start to think about what the Gate voltage is and how that may affect the circuit.

2. We are talking about frequency response so that means we are probably going to want to draw the small signal equivalent circuit.

Remember that the capacitors $C_1$and C_2will act like short circuits at high frequencies so we will ignore them, but we will have to account for some of the capacitance internal to the device.

Both devices have internal capacitances that are very similar. As you can see from the small signal models for a MOSFET (above) and BJT (below), the only significant difference is that the BJT has an additional resistance Rpi between the Base and Emitter.

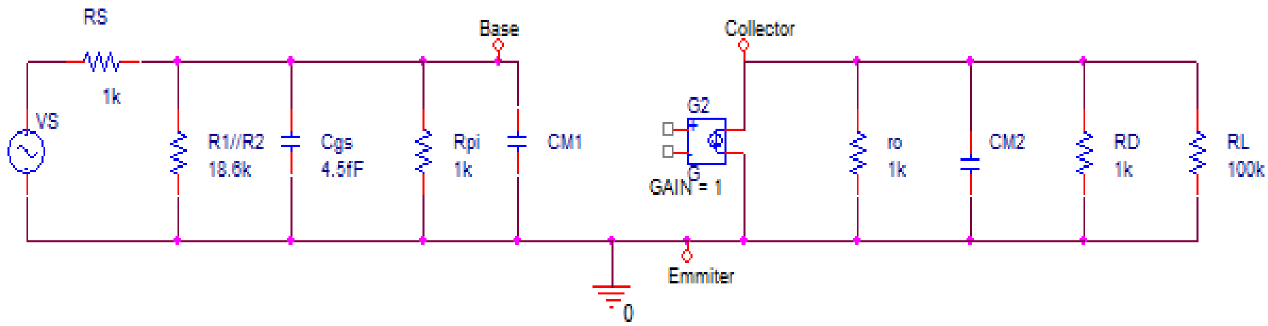
Most of the analysis we will do is based on the small signal model. Note that small signal models are not typically used in PSPICE so this picture may look a bit odd, especially the controlled source but for our purpose it is good to have a visual reference. To start we will point out what everything is. Cgs is an internal capacitance



betwe

en the gate and source. The

values for Cgs was similar to one the a PSPICE simulation may give. CM1 and CM2 are Miller capacitances which we will find values for



later

4.RLC circuits and their response.

The RLC circuit which provides nearly undamped oscillations is called ringing circuit. Consider a R-L-C circuit is as shown below:

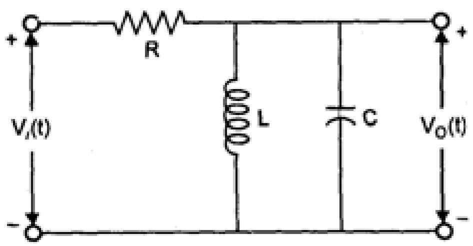


Fig. The RLC ckt.

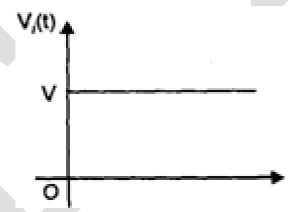


Fig. The step input

We can combine the parallel combination of the inductor 'L' and the capacitor 'C' into impedance 'Z'.

$$Z = \frac{SL\left(\frac{1}{SC}\right)}{sL + \frac{1}{sC}} = \frac{sL}{1+s^2LC}$$

$$I(s) = \frac{V_i(s)}{R+Z}$$

$$V_0(s) = I(s).Z = \frac{V_i(s).z}{R+Z}$$

$$\frac{V_0(s)}{V_i(s)} = \frac{Z}{R+Z} = \left[\frac{\frac{sL}{1+s^2LC}}{R+\frac{sL}{1+s^2LC}}\right]$$

$$\frac{V_0(s)}{V_i(s)} = \frac{sL}{R(1+s^2LC)+sL} = \left[\frac{sL}{RLCs^2+Ls+R}\right]$$

$$G(s) = \left[\frac{sL}{RLCs^2+Ls+R}\right] \qquad ...(i)$$

The ratio G(s) is known as the transfer function of the circuit. The characteristics equation of the circuit can be written by equating the denominator polynomial of G(s) o zero as shown in equation (ii)

$$RLCs^2 + Ls + R = 0 \qquad \text{...(ii)}$$

$$s = \frac{-L \pm \sqrt{L^2 - 4R^2LC}}{2RLC} \qquad \text{...(iii)}$$

$$s = -\frac{1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}} \qquad \text{... (iv)}$$

This is a quadratic equation –which can be solved to find its roots, 's_1' and 's_2'. The poles of the transfer function G(s) are same as the roots of the characteristic equation 's_1' and 's_2'.

Let us introduce the dumping constant 'k' and undamped period by equation (v) and (vi)

And

$$k = \frac{1}{2R} \cdot \sqrt{\frac{L}{C}} \qquad \text{...(v)}$$

$$T_0 = 2\pi\sqrt{LC} \qquad \text{...(vi)}$$

When we introduce these value in equation (i) we obtain the following form,

$$s = \frac{-2\pi k}{T_0} \pm j \cdot \frac{2\pi}{T_0} \sqrt{1-k^2}$$

We can see that roots are, purely imaginary, $s = \pm j \cdot \frac{2\pi}{T_0}$.

In this case, the response is an un-damped sinusoidal waveform of period T_0. If k = 1, we can see that the roots are equal, corresponding to the critically damped case.

If k> 1, there would not be any oscillations in the output waveform and the response is said to be over-damped. If k < 1, the output would be a sinusoidal waveform whose amplitude decays with time and the response is said to be under-damped.

The quality factor of the RLC circuit can be written as equation (vii).

$$Q = w_0 RC \qquad \text{... (vii).}$$

We have already defined the damping constant as

$$k = \frac{1}{2R} \cdot \sqrt{\frac{L}{C}}$$

We can verify that,

$$Q = w_0 RC = \frac{2\pi RC}{T_0} = \frac{RC}{\sqrt{LC}} = R \cdot \sqrt{\frac{C}{L}} = \frac{1}{2k}$$

$$Q = \frac{1}{2k} \qquad \text{...(viii)}$$

$$k = \frac{1}{2Q} \qquad \text{...(ix)}$$

Now we can see that the damping constant 'k' is inversely proportional to the quality factor 'Q'. Now, we can write the transfer function a (s) written as equation (i) in the following form.
Equation (x)

$$G(s) = \frac{sL}{(s-s_1)(s-s_2)} \quad ...(x)$$

We already know as indicated in equation (v) that the poles of the transfer function G(s) are same as the roots of the characteristic equation 's_1' and 's_2'.

$$s_1 = -\frac{2\pi k}{T_0} + j.\frac{2\pi}{T_0}.\sqrt{1-k^2}$$

$$s_2 = -\frac{2\pi k}{T_0} - j.\frac{2\pi}{T_0}.\sqrt{1-k^2}$$

Response of the RLC circuit to a step waveform:
The input to this RLC circuit is a step waveform defined below. This waveform is plotted in Fig. (i)(b)

$$v(t) = \begin{cases} 0 & \text{for } t < 0 \\ V & \text{for } t \geq 0, \end{cases}$$

We know the L.T. of the step waveform

$$v_i(s) = \left[\frac{V}{s}\right]$$

Employing this relation, following equation can be written as

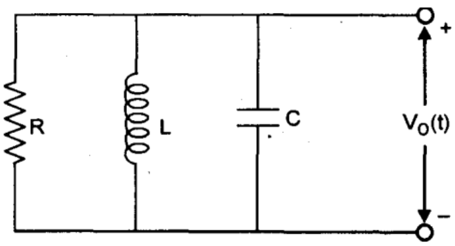
$$\frac{v_0(s)}{v_i(\Delta)} = \left[\frac{sL}{RLC\,s^2 + Ls + R}\right]$$

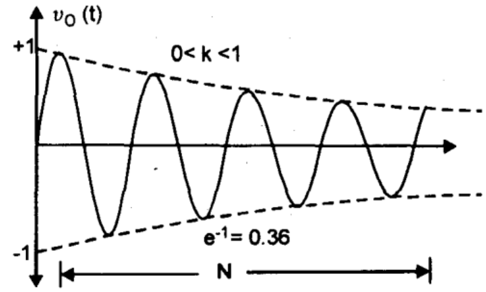
$$\frac{v_0(s)}{v/s} = \left[\frac{L}{RLC\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)}\right]$$

$$\frac{V_0(s)}{V} = \left[\frac{L}{RC\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)}\right]$$

$$\frac{v_0(s)}{V} = \frac{1}{RC\,(s-s_1)(s-s_2)} \quad ...(xi)$$

Where 's_1' and 's_2' are the roots of 's'.
Slow-decay under-damped Oscillatory Response: —
In this kind of response 'k' is +ve but far less than '1'. In other words, k<<1 and close to zero. Since there is almost no damping in this case, the output response would closely resemble a sinusoidal waveform.





1. RLC circuit functioning (b) Response of the ringing ckt.

as a ringing circuit.

Fig.2. RLC circuit functioning as a ringing circuit.

The damping constant 'k' is +ive close to zero. Making use of the relation k = 0, we find that both the roots become imaginary

$$s_1 = j.\frac{2\pi}{T_0} \text{ and } s_2 = -j.\frac{2\pi}{T_0}.$$

The RLC circuit shown in Fig. 2(a) operating in this condition is popularly known as the ringing circuit. A typical output response for this case is indicated in Fig. 2(b)

5.Diode as Logic gate

A diode is a two-terminal electrical device that allows current to flow in one direction but not the other. It is like a pipe with an internal valve that allows water to flow freely in one direction but shuts down if the water tries to flow backward. The schematic diagram for a diode is shown in Figure B.5.

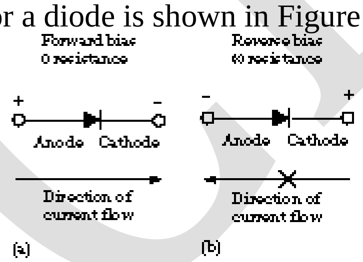


Figure B.5 Diode operation

The diode's two terminals are called the anode and cathode. In the diode symbol, the arrow points from the anode（flat part of triangle）toward the cathode（point of the triangle）.

The device operates by allowing current to flow from anode to cathode, basically in the direction of the triangle. Recall that current is defined to flow from the more positive voltage toward the more negative voltage（electrons flow in the opposite direction）. If the diode's anode is at a higher voltage than the cathode, the diode is said to be forward biased, its resistance is very low, and current flows. The diode is not a perfect conductor, so there is a small voltage drop, approximately 0.7 V, across it. If the anode is at a lower voltage than the cathode, the diode is reverse biased, its resistance is very high, and no current flows.

We can construct simple gates with nothing more than two or more diodes and a resistor. See Figure B.6.

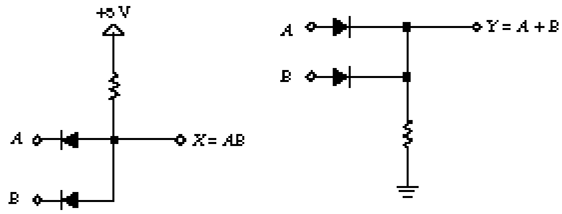


Figure B.6 Simple gates from diodes and resistors.

At the left of the figure is a diode AND gate, and at the right a diode OR gate. Let's examine the AND gate first. If one of the inputs *A* or *B* is grounded, current flows through the diode and the output node *X* is at a low voltage. The only way to get a high output is by having both inputs high. This is clearly a logical AND function.

Now we turn to the OR gate. Whenever one or the other of the inputs *A* and *B* are high, current flows through the associated diode. This brings the output node *Y* to a high voltage. This circuit clearly implements a logical OR.

16. University previous Question papers

Code No: R09220203 R09

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B. Tech II Year - II Semester Examinations, November/December 2012

ELECTRONIC CIRCUITS

(Electrical and Electronics Engineering)

Time: 3 hours

Answer any five questions
All questions carry equal marks

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1. Explain the analysis of a Common Collector Amplifier using simplified Hybrid Model. [15]

2.a) Verify that the negative feedback in an amplifier improves its band width, and its stability.
b) The output power of an amplifier is 100 watts, when the load resistance is 10 Ω. The harmonic distortion in the output is 4%. Determine the voltage gain, if the input is 2volts. What is the required feedback ratio, if the harmonic distortion is to be restricted to 0.02%. [10+5]

3.a) Give the topology of a Current shunt feedback amplifier and derive the expressions for its voltage gain, input impedance, and output impedance.
b) An amplifier has a voltage gain of 50 and a band width of 100KHz. In order to increase its band width, 1% negative feedback is introduced. Find the bandwidth with feedback. [12+3]

4.a) Derive the expression for the frequency of oscillation of a Wein Bridge Oscillator.
b) In a Colpitts oscillator, the capacitors, C1=1nF; C2=10nF; and L=110μH. Find the feedback factor and operating frequency. [10+5]

5.a) Derive the expression for the efficiency of a Transformer Coupled Class A amplifier.
b) A power amplifier has an input signal of 0.4Sinωt, at a frequency of 100KHz. Output current of the amplifier is found to be 5Sinωt+0.9Sin2ωt+0.6Sin4ωt+0.01Sin5ωt. Find the total harmonic distortion. [10+5]

6. A 10Hz symmetrical square wave, whose peak to peak amplitude is 2volts, is impressed upon an RC High Pass circuit, whose lower 3dB frequency is 5Hz. Calculate and sketch the output wave form, and find the peak to peak voltage of the output. [15]

7.a) Explain, how a BJT acts as a Clipper. Draw the necessary wave forms.
b) Explain about various switching times of a BJT. [7+8]

8.a) Explain the operation of an Emitter coupled Bi-Stable Multi-vibr[illegible]
b) Write about symmetrical and Un-symmetrical Triggering of Mul[illegible]

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6.a) Compare the unidirectional and bidirectional sampling gates.
b) Draw the circuit diagram of six-diode sampling gate and explain its working. [5+10]

7.a) Explain the frequency division with respect to a sweep circuit.
b) Explain working of monostble relaxation device as a divider. [7+8]

8.a) Draw the circuit diagram of AND gate using diodes and explain its working.
b) Explain the working of TTL NAND gate with suitable circuit diagram. [7+8]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)
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1. For the amplifier circuit shown with partially unbypassed emitter resistance, calculate the voltage gain with R_4 in place and with R_4 shorted. Consider h_{ie} = 1.1KΩ, h_{fe} = 100, h_{re} & h_{oe} are negligibly small. Assume R_1 and R_2 to be 100KΩ and 22 KΩ respectively.

b) Analyse what the output voltage should be if the DC power supply given to a CE amplifier is shorted to ground. [10+5]

2.a) With the help of circuit diagram and equivalent circuit of a Darlington amplifier generate the expression for the overall input impedance of the pair.
b) Develop a generalized expression for overall current gain(A_{IS}) when two transistor stages with $R_{OUT2} < R_L$, $R_{OUT1} > R_{IN2}$, $R_{IN1} > R_S$ and individual voltage gains are A_{V1}, A_{V2}. [7+8]

3.a) A transistor amplifier in CE configuration is operated at high frequency with the following specifications. f_T=6MHz, g_m=0.04,h_{fe} =50, $r_{bb'}$ =100 Ω, R_s =500 Ω , $C_{b'c}$ =10pF, R_L=100 Ω. Compute the voltage gain, upper 3dB cut-off frequency, and gain bandwidth product (GBW).
b) Derive an expression for the overall higher cut-off frequency of a two stage amplifier with identical stages of individual higher cut-off frequency, f_H. [7+8]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a). If the non-linear distortion in a negative feedback amplifier with an open loop gain of 100 is reduced from 40% to 10%with feedback, compute the feedback factor, β of the amplifier.
b) Draw the circuit diagram of a current series feedback amplifier, Derive expressions to show the effect of negative feedback on input & output impedances, bandwidth, distortion of the amplifier. [6+9]

6.a) Differentiate between RC and LC type oscillators.
b) Derive the expression for frequency of oscillation in a Hartley Oscillator.
c) State Barkhausen Critterion for Oscillations [5+7+3]

7.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.

b) What are the drawbacks of transformer coupled power amplifiers?

c) A push pull amplifier utilizes a transformer whose primary has a total of 160 turns and whose secondary has 40 turns. It must be capable of delivering 40W to an 8 Ω load under maximum power conditions. What is the minimum possible value of V_{cc}?

[5+4+6]

8.a) List possible configurations of tuned amplifiers.

b) Derive an expression for bandwidth of a capacitive coupled tuned amplifier in CE configuration. Make necessary assumptions and mention them. [6+9]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

Answer any FIVE questions

All Questions Carry Equal Marks

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1.a) For the common emitter amplifier shown, draw the AC and DC load lines. Determine the peak-to-peak output voltage for a sinusoidal input voltage of 30mV peak-to-peak. Assume C_1, C_2 and C_3 are large enough to act as short circuit at the input frequency. Consider h_{ie} = 1.1KΩ, h_{fe} = 100, h_{re} & h_{oe} are negligibly small.

b) State Miller's theorem. Specify its relevance in the analysis of a BJT amplifier.

c) Write expressions for A_V and R_{IN} of a Common Emitter amplifier. [7+4+4]

2.a) Derive expressions for overall voltage gain and overall current gain of a two-stage RC coupled amplifier.

b) List out the special features of Darlington pair and cascode amplifiers. [9+6]

3.a) Discuss the effect of emitter bypass capacitor and input & output coupling capacitors on the lower cut-off frequency if number of amplifiers are cascaded.

b) Describe how an emitter follower behaves at high frequencies. [8+7]

4.a) Discuss the effect of different types of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) The β and the open loop gain of an amplifier are -10% and -80 respectively. By how much % the closed loop gain changes if the open loop gain increases by 25%?

b) Compare the characteristics of feedback amplifiers in all the four configurations.

c) Reason out why 2 stages are required to implement current shunt feedback. [5+6+4]

6. Starting from the description of a generalized oscillator, derive the expression for frequency of oscillation in a colpitts oscillator. [15]

7.a) With the help of a suitable circuit diagram, show that the maximum conversion efficiency of a class B power amplifier is 78.5%.

b) Explain how Total harmonic distortion can be reduced in a Class B push-pull configured amplifier. [7+8]

8.a) Derive an expression for the bandwidth of a synchronous tuned circuit.

b) Discuss the necessity of stabilization circuits in tuned amplifiers. [8+7]

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Code No: R09220403 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, May-2013
Pulse and Digital Circuits
(Common to ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Compare linear wave shaping with non-linear wave shaping.
b) A symmetrical square wave of peak-to-peak amplitude 'V' and frequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by

$$P = \frac{1 - e^{-1/2RCf}}{1 + e^{-1/2RCf}} \times 100\%$$

[7+8]

2.a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.
b) Explain the effect of diode characteristics on clamping voltage. [8+7]

3. Write short notes on:
a) Diode switching times
b) Switching characteristics of transistors
c) FET as a switch. [4+7+4]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and base of both transistors. [15]

5.a) Why the time base generators are called sweep circuits? Write the differences between the voltage and current time base generators?
b) With neat sketches and necessary expressions, explain the transistor Miller time-base generator. [9+6]

6.a) With the help of a neat diagram, explain the working of four-diode sampling gate. Derive expressions for its gain(A) and V_{min}.
b) Explain the application of sampling gate in a sampling scope. [10+5]

7.a) With the help of a neat circuit diagram and waveforms explain synchronization of a sweep generator with pulse signals.
b) Compare sine-wave synchronization with pulse synchronization. [8+7]

8.a) Realize a three-input NAND gate using Transistor-Transistor Logic. Explain its operation with Totem-pole load.
b) With reference to logic gates, explain the terms:
(i) Fan-out, (ii) Noise Margin, (iii) Propagation Delay, (iv) Figure of Merit. [7+8]

17. Question Bank

UNIT 1: Single Stage Amplifiers

1. Explain the classification of amplifiers?
2. Draw the circuit of CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?
3. Draw the circuit of CE amplifier with un bypassed emitter resistor and derive expressions for Ri, Ro ,Av &Ai using approximate h-parameter model?
4. Draw the circuit of CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?
5. Compare different types of amplifier circuits?
6. Explain the term multistage amplifiers & its advantages?
7. Draw the circuit of two stage RC coupled CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?
8. Draw the circuit of cascade CB-CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?
9. Draw the circuit of CC- CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?
10. Draw the circuit of Darlington CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model and its merits &demerits ?

Part-B FeedBack Amplifiers

11. . Show that for voltage shunt feedback amplifier transresistance gain R_i and R_o are decreased by a factor (1+Aβ) with feedback?
12. Explain the concept of feedback with block diagram applied to an amplifier circuit. What are the advantages and disadvantages of positive & negative feedback?
13. Draw the circuit diagram of current shunt feedback amplifier and expressions for R_{if} and R_{of}?
14. Draw the frequency response of an amplifier with &without feedback and show the bandwidth for each case and how these two curves are related?
15. Draw the circuit diagram of voltage series feedback amplifier and expressions for R_{if} and R_{of}?
16. Explain the concept of positive feedback used in oscillators. State and explain Barkhausen criterion?

17. Show that the gain of Wien bridge oscillator using BJT amplifier must be at least **3** for the oscillations to occur?

18.Explain the basic circuit of an LC oscillator and derive the conditions for the oscillations?

19. What are the factors that affect frequency stability of an oscillator? How frequency stability improved in oscillators?

20. Draw the circuit diagram of RC phase shift oscillator using BJT.derive the expression for frequency of oscillatoions?

UNIT 2: Frequency Response of BJT and FET

1. What is frequency response and explain how it is obtained?

2. Explain the relation between low frequency gain &mid frequency gain with suitable expres

sions?

3. Explain the terms B.W, cutoff frequencies of an amplifier circuit?

4. Draw the equivalent circuit of a transistor at high frequencies(i.e) hybrid π model?

5. Explain Gain-bandwidth product for voltage &current?

6. Explain small signal model of a MOS transistor its equivalent circuit?

7. Explain the circuit of CS amplifier with resistive load using small signal model?

8. Explain the circuit of CS amplifier with diode connected load using small signal model?

9. Explain common gate amplifier circuit and derive expressions for Ri, Ro &Av?

10. Draw the circuit for folded cascade amplifier and explain its analysis using small signal model?

UNIT 3:

Part-A Multivibrators

1. What is a Bistable circuit? What are the other names of a bistable multivibrator?
2. What are the applications of a bistable multivibrator?
3. What do you mean by the term ‘loop gain’?
4. Explain how a constant output swing can be obtained in a binary?
5. What are the commutating capacitors? Why these are used in binary?
6. What do you mean by transition time? How it can be reduced?
7. Define the resolving time, settling time and resolution time.

8. What are the methods of improving the resolution of a binary?
9. Explain the working of non-saturated binary.
10. What is a non saturated binary? What are the advantages and disadvantages of it?
11. Compare the saturated and non-saturated binary.
12. What is unsymmetrical triggering ? where is it used?
13. What is necessity of triggering ? What are the different types of triggering?
14. Compare symmetrical and unsymmetrical triggering.
15. Explain any one method of unsymmetrical triggering of a binary?
16. Explain any one method of symmetrical triggering of a binary?
17. What are the advantages and disadvantages of a direct-connected binary?
18. What is a Schmitt trigger? What are the applications of it.
19. With the help of neat circuit diagram and waveforms, explain the working of a Schmitt trigger.
20. Define the terms upper triggering point and lower triggering point with the help of waveforms
21. How can hysteresis be eliminated in a Schmitt trigger?
22. Define the terms: stable state, quasi stable state, dc coupling and ac coupling
23. Compare ac coupling and dc coupling in Multivibrator.
24. Define the terms UTP and LTP of a Schmitt trigger and explain how these are varied?
25. Why is monostable multivibrator also called a gating circuit and give its applications.
26. Why is monostable multivibrator also called a delay circuit and draw its circuit diagram.
27. With the help of neat circuit diagram explain the working of a collector coupled Monostable multivibrator.
28. Derive an expression for the gate width of monostable multivibrator.
29. Derive the expression for the gate width of a monostable multivibrator considering the effect of reverse saturation current.
30. What type of triggering is used in a monostable multivibrator? Draw the circuit of it.

Part-B

Clippers & Clamppers

1. What are the clipping circuits? Give some examples?
2. How the clipping circuits are used in non-linear wave shaping?
3. Why should the resistance in the clipping circuit be chosen as the geometric mean of the diode forward and reverse resistances?
4. What is the disadvantage of having a diode as a series element in a clipper?
5. What are the other names of clipping circuits?
6. With the help of a neat circuit diagram, explain the working of an emitter-coupled clipper.
7. What is a comparator? How it is used?
8. Distinguish between comparators and clipping circuits.
9. What are the applications of voltage comparators?
10. What is the disadvantage of having a diode as a shunt element in a clipper?
11. What do you mean by a regenerative comparator? Give an example.
12. What do you mean by a non-regenerative comparator? Give an example
13. Draw a circuit to transmit that part of a sine wave which is below +6V and explain its working

14. Draw a circuit to transmit that part of a sine wave which is below -5V and explain its working
15. Draw a circuit to transmit that part of a sine wave which lies between +4V and +8V and explain its working
16. Draw a circuit to transmit that part of a sine wave which lies -3V and +6V and explain its working
17. Draw a circuit to transmit that part of a sine wave which lies between -4V and -7V and explain its working
18. Draw the emitter coupled clipper circuit and explain its operation
19. What do you mean by a two-way clamp and how it differ for one-way clamp?
20. What is clamper? How it is used in Non-linear wave shaping?
21. Why is clamping circuit also called dc inserter?
22. What do you mean by clamping? What the other names of a clamping circuit?
23. What is positive clamping and explain it with suitable circuit.
24. What is negative clamping and explain it with suitable circuit.
25. Derive the relation between the tilts in the forward and reverse directions of the output of a clamping circuit excited by a square-wave input.
26. State and prove the clamping circuit theorem
27. What is the difference between clamping and clamping?
28. What do you mean by biased clamping?
29. What are the limitations of practical clamping circuit?
30. What do you mean by biased clamping?

UNIT 4:

Part-A

1. Explain about class A, class B, class C and class AB operation of power amplifiers?

2. Draw the circuit diagram of complementary symmetry push pull amplifier and its working?

3. Distinguish between crossover distortion and harmonic distortion. How they can be eliminated?

4. Show that the efficiency of class A amplifier is 50%?

5. Explain the concept of heat sinks?

PART-B

1. What is linear wave shaping? Give some examples.
2. Draw the low pass RC circuit and explain its working.
3. How a Low Pass RC circuit is used in linear wave shaping?
4. Find the lower cut of frequency of a low-pass circuit?
5. Derive an expression for the upper cut-off frequency of a low pass circuit.
6. Derive an expression for the output of low pass circuit excited by a step input.
7. Derive an expression for the rise time of the output of a low-pass circuit excited by a step input
8. Define the rise time and write the expression of it.
9. How does a low-pass circuit reserve the pulse shape?

10. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input
11. Derive an expression for the output of a low-pass circuit excited by an exponential input.
12. Explain how a low pass circuit acts as an integrator?
13. Show that low-pass circuit with a large time constant acts as an integrator.
14. Draw the response of a low pass circuit with small, medium and large time constants when input is square wave.
15. Draw the high-pass circuit and explain its working.
16. How a High RC circuit is used in linear wave shaping?
17. Find the upper cut of frequency of a high-pass circuit?
18. Derive an expression for the lower cut-off frequency of a High pass circuit.
19. Derive an expression for the output of high pass circuit excited by a step input.
20. Derive an expression for the rise time of the output of a high-pass circuit excited by a step input
21. How does a high-pass circuit reserve the pulse shape?
22. Derive an expression for the output voltage levels under steady state conditions of a high pass circuit excited by a ramp input
23. Derive an expression for the output of a high-pass circuit excited by an exponential input.
24. Explain how a high pass circuit acts as a differentiator?
25. Draw the response of a High pass circuit with small, medium and large time constants when input is square wave.
26. Why the capacitor in an RC high-pass circuit is called a blocking capacitor?
27. Which type of RC circuit is called a capacitive coupling circuit? Draw the circuit diagram of it.
28. What must be the time constant of a high-pas circuit for the output to be in the form of a tilt for a square wave input?
29. What must be the time constant for a high pass circuit for the output to be in the form of spikes for a square wave input?
30. Derive an expression for the percentage tilt of the output of a high pass circuit with large time constant excited by a symmetrical square wav with zero average value.

UNIT 5:

1. Name the devices that can be used as switches.
2. Define a storage time and transition time of a diode
3. Explain how a diode act as a switch?
4. Define a diode forward recovery time and reverse recovery time.
5. Explain how a transistor acts as a switch?
6. When does a transistor act as a closed switch and an open switch?
7. Define a rise time and fall time of a transistor switch.
8. What is delay time and storage time of a transistor? What factors does contribute to it?
9. Write a short notes on a diode switching times.
10. Write a short notes on a transistor switching times.

11. A rectangular pulse of voltage is applied to the base of a transistor driving it from cut-off to saturation. Discuss the various times involved in the switching process.
12. How are the junctions of a transistor biased for cut-ff, active and saturation regions of operations?
13. Prove that the total turn-on time of a transistor is the sum of the delay time and the rise time.
14. Explain how a transistor acts as a closed switch in saturation region?
15. Explain how a transistor acts as a open switch in cut off region?
16. Draw and Explain the piece-wise linear characteristics of a diode.
17. Explain briefly about the breakdown voltages of a transistor.
18. Define collector to emitter breakdown voltage and Write its equation in terms of hFE.
19. For an npn Ge transistor(n=6 , hFE=50) and BVCBO is about 20V /Find the collector to emitter breakdown voltage?
20. Explain the design procedure of Transistor Switch.
21. For a CE transistor circuit with VCC = 15V, Rc=1.5K ohms, calculate the transistor power dissipation at open and closed positions.
22. Explain the variation of saturation parameters of transistor with temperature?
23. Explain the variation of VBE(sat) and VCE(sat) of transistor with temperature.
24. For a common emitter circuit, Vcc = 15V , RC =1.5Kohms and IB=0.3mA. Determine the value of hFE(min) for saturation to occur.
25. Sketch the typical transistor common-emitter characteristics. Identify the various regions of the characteristics and show how VCE(sat) differs with different load resistances.
26. A common emitter circuit has Vcc=20V and a collector resistor which can be either 20Konms to 2Kohms. Calculate the minimum level of base current to achieve saturation in each case.
27. Derive the expression for fall time of transistor switch.
28. Derive the expression for rise time of transistor switch.
29. Draw the collector waveform of transistor switch and indicate all the time intervals.
30. What the factors that contribute the delay time of transistor switch?
31. Define the storage time constant and how it is related to storage time of transistor switch?

18. Assignment topics

UNIT 1

Part A:

1. Explain the basic amplifier circuit and its components?

2. Using hybrid model explain the circuit of CB amplifier and derive expressions for Ri, Ro ,Av &Ai ?

3. Draw the circuit of CE amplifier with un bypassed emitter resistor and derive expressions for Ri, Ro ,Av &Ai using approximate h-parameter model?

4. Draw the circuit of CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

5. Compare different types of amplifier circuits?

Part B:

Show that for voltage shunt feedback amplifier transresistance gain R_i and R_o are decreased by a factor $(1+A\beta)$ with feedback?

2. Explain the concept of feedback with block diagram applied to an amplifier circuit. What are the advantages and disadvantages of positive & negative feedback?

3. Draw the circuit diagram of current shunt feedback amplifier and expressions for R_{if} and R_{of}?

4. Draw the frequency response of an amplifier with &without feedback and show the bandwidth for each case and how these two curves are related?

5. Draw the circuit diagram of voltage series feedback amplifier and expressions for R_{if} and R_{of}?

UNIT 2

Part A:

1. Explain the frequency response of single stage amplifier?
2. Derive the expressions for lower& upper cutoff frequencies?
3. Explain the terms B.W, cutoff frequencies of an amplifier circuit?
4. Draw the equivalent circuit of a transistor at high frequencies (i.e) hybrid π model?
5. Explain Gain-bandwidth product for voltage &current?
6. Explain small signal model of a MOS transistor its equivalent circuit?
7. Explain the circuit of CS amplifier with resistive load using small signal model?
8. Explain the circuit of CS amplifier with diode connected load using small signal model?
9. Explain common gate amplifier circuit and derive expressions for Ri, Ro &Av?
10. Draw the circuit for folded cascade amplifier and explain its analysis using small signal model?

UNIT 3

Part A:

1. What is monostable multivibrator? Explain with the help of neat circuit diagram the principle of operation of monostable multivibrator, and derive the expression for pulse width. Draw the waveforms at collector and base of the both transistors.
2. a) Draw the circuit of bi-stable multivibrator with symmetrical collector triggering.
   b) Write the applications bistable and monostable multivibrators
3. a) Draw the circuit diagram of Astable multivibrator to obtain the frequency division by 5. Explain its working with waveforms.

b) Why collector catching diodes are used in multivibrators?

4. Explain and explain the operation of Schmitt trigger with neat sketches, and derive the expressions for UTP and LTP.
1. Design a monostable multivibrator circuit that produces a pulse width of 10ms. Assume hfe= 30, $V_{CE(sat)=}$0.3V, $V_{BE(sat)=}$ 0.7V, $I_{c(sat)=}$5mA, V_{cc}=6V, V_{BB}= -1.5V.

Part B:

1. a. what is non-linear wave shaping? What is clipping ? Explain the operation of below mentioned circuits with circuit diagrams, transfer characteristics and waveforms i) series positive clipper with and without V_R. ii) Shunt negative clipper with and without V_R.
b) For a 2-level clipper with peak input 100V and forward bias diode reference voltage 75V and reverse bias diode reference voltage 50V, sketch the transfer characteristics, input and output voltage waveforms. Consider the diodes as ideal.

2. Explain the operation of transistor clippers (common emitter type and emitter follower type) with neat sketches.
3. a. What is clamping operation? Explain the operation of biased positive peak clamper with output waveforms.
b. What is the effect of source resistance and the diode resistance in clamping circuits?

4. a. State and prove clamping circuit theorem.
b. Draw the output waveform of a practical clamping circuit when a square wave is given as input. Derive the relation between Δ_f and Δ_r in this case.

5. a) What is synchronized clamping? Draw the circuit and explain its operation.
b) Explain the operation of diode comparator. Briefly mention various applications of comparators.

UNIT 4

1. Explain about class A, class B, class C and class AB operation of power amplifiers?

2. Draw the circuit diagram of complementary symmetry push pull amplifier and its working?

3. Distinguish between crossover distortion and harmonic distortion. How they can be eliminated?

4. Show that the efficiency of class A amplifier is 50%?

5. Explain the concept of heat sinks?

6. Derive the output equations and draw the output wave forms of a RC low pass circuit for the pulse and the square waveform inputs.
7. How an RC low pass circuit works as an integrator?
8. a). Derive the expression for percentage tilt P of a square wave output of a RC high pass circuit.
9. b). Why compensation is required in attenuator circuits? Derive the expression for perfect compensation.

10. A 100 Hz square wave is fed to an RC circuit. Calculate and plot the waveform under the following conditions, The lower 3-dB frequency is 1) 3 Hz 2) 30 Hz 3)300 Hz

UNIT 5

1. . How the minority carriers are distributed in a p-n junction diode during forward biased condition and the reverse biased condition.
   b. Draw the Ideal and piecewise linear model diode characteristics and explain.
2. a. Explain the operation of a diode as switch. What is reverse recovery time, storage time and transition time of a diode? Draw the switching characteristics of the diode along with t_{rr}, t_s and t_t timings.
   b. Explain Zener break down(Zener diode) and Avalanche break down(PN junction diode) mechanisms.
3. a. Explain the operation of a transistor as switch with its switching characteristics.
   b. Define the following for transistor switch

i) Rise time ii) Fall time iii) Storage time iv) Delay time v) Switch ON time

vi) Switch OFF time

4. a. Explain the breakdown voltage consideration of transistor. Derive expression for BV_{CEO} in terms of BV_{CBO}.
   b. Explain the saturation parameters of transistor and their variations with temperature.
5. a. Explain the operation of Silicon Controlled Switch (SCS) and give its applications.
   b. Calculate the min ß required for a fixed bias common emitter Si transistor, where V_{CC}=10V, R_c= 1 KΩ, R_b= 10 K Ω, Vi= a square wave of 5V peak to peak. Draw the circuit.

19. Unit-wise Quiz Questions and long answer questions

Unit-1

Unit 1:

1) Critical capacitance with smallest equivalent resistance that determines the lower cut off of CB amplifier is
a) I/P coupling capacitor
b) Emitter bypass capacitor if c1 = c2
c) c2 output coupling capacitor
d) None.

2).resultant phase shift of odd no of CE amplifier stages at mid band frequency is
a)3600
b) 1800
c) 450
d) 900

3).he miller input capacitance in CB AMP IS
a) large compared to miller capacitance in CE
b) very large because of +ve voltage gain in CB
c) small because of +ve voltage gain in CB
d) is not negligible compare to other capacitance

4) Identify the correct statement regarding the voltage gain of a CE transistor amplifier
a) it increases with increase in ac load R
b) it is independent of ac load R & is large
c) it decreases with increase in ac load R
d) it is always approximately unity

5) Identify the incorrect statement
[d]
a) frequency distortion in an amplifier is mainly due to the reactive component circuit
b) amplitude distortion is also referred to as non-linear distortion
c) distortion in amplifier due to unequal phase shifts at different frequencies is called delay distortion
d) phase shift distortion is same as frequency distortion
ans: [D]

6) i/p &o/p capacitors in a transistors amplifier are not referred to as
[a]
a) inter electrode capacitors
b) coupling capacitors
c) blocking capacitors
d) dc de-coupling capacitors
ans : [A]

7) CB amplifier of BJT is similar in behaviour with following FET configuration
[a]
a)common gate amplifier
b) common drain amplifier
C) common source amplifier
d)swamped source resistor amplifier
ans:[A]

8) The miller i/p capacitance in CB amplifier
[c]
a) Is large compared to miller capacitance in CE
b) is very large because of +ve voltage gain in CB
c) is small because of +ve voltage gain in CB
d) not negligible compared to other capacitance
ans: [C]

9) CE is the capacitance of forward biased junction & is therefore
[c]
a) independent of collector current
b) much lager than Cc
c) mainly diffusion capacitance
d) mainly transition capacitance
ans: [C]

10) dissipation capability of a transistor is defined as
[a]
a) capability to launch heat generated into the surroundings
b) deviation in power delivered to load resistor
c) capability to withstand the variation in dc power at operating power
d) deviation in o/p & i/p signal wave shapes
ans: [A]

11) phase difference between o/p voltage &i/p voltage of a CC amplifier at mid band frequencies
[b]
a) 1800
b) 00
c) 450
d) 900
ans : [B]

12) major draw back of Darlington transistor pair
[d]
a) low current gain compared to single emitter follower
b) dependence of Av on transistor selected
c) low i/p impedance compared to single emitter follower
d) dependence of H -parameters on quiescent conditions

ans: [D]

13) cascade amplifier is 2- transistor combination has
a) collector of first transistor is connected to the base of second transistor
b) collector current of first transistor is same as emitter current of second transistor
c) emitter current of first transistor is same as the collector current of the second transistor
d) none

14) resultant phase shift of odd no of CE amplifier stages at mid band frequency is a) 3600
b) 1800
c) 450
d) 900

15) major drawbacks of Darlington transistor pair is
a) low current gain compared to single emitter follower
b) dependence of AV on transistor selected condition
c) low i /p impedance compared to single emitter follower
d) dependence of h-parameters on quiescent point.

16) Resultant current gain of a Darlington pair individual current gain of hfe is [d]
a) hfe/2
b) hfe
c) 2hfe
d) hfe2
ans: [D]

17) 2-stage rc coupled amplifier is configured as [a]
a) 2 capacitively coupled CE stages cascaded
b) a CE stage capacitively coupled to a CC stage
c) 2 capacitively coupled CB stages cascaded.
d) 2 capacitively coupled CC stages cascaded
ans: [A]

18) 2-transistor cascade with both collectors tied together & emitter of the transistor connected to the base of the transistor is referred to as [a]
a) Darlington pair
b) CE &CC cascade
c) cascade amplifier
d) differential pair
ans: [A]

19) the i/p impedance of cascade amplifier is [b]
a) hic
b) hie

c) infinity
d) hib
ans: [B]

20) type of inter stage coupling resulting in highest overall gain
[c]
a) direct coupling
b)inductive coupling
c) RC coupling
d) transistor coupling
ans : [C]

21) main disadvantage of Darlington pair amplifier is
[d]
a) low i/p impedance
b) low current gain
c) high o/p impedance
d)high leakage current
ans: [D]

22) Major advantage of boot strap Darlington pair over single Darlington pair is
(a) High overall Av with proper DC biasing
(b) increased Ai irrespective of bias condition
(c) high i/p impedance irrespective of bias condition
(d) increased Ai depending upon the bias condition
Ans: (c)

Feed Back Amplifiers

1. When negative voltage feedback is applied
to an amplifier, its voltage gain ....
   (i) is increased
   (ii) (ii) is reduced
   (iii) remains the same
   (iv) none of the above
2. The value of negative feedback fraction is
always ....
   (i) less than 1
   (ii) (ii) more than 1
   (iii) equal to 1
   (iv) (iv) none of the above
3. If the output of an amplifier is 10 V and 100 mV from the output is fed back to the
input, then feedback fraction is ....
   (i) 10
   (ii) 0.1
   (iii)0.01
   (iv)(iv) 0.15
4. The gain of an amplifier without feedback
is 100 db. If a negative feedback of 3 db is

applied, the gain of the amplifier will become ....
(i) 101.5 db
(ii) 300 db
(iii) 103 db
(iv) 97 db
5. If the feedback fraction of an amplifier is 0.01, then voltage gain with negative voltage feedback is approximately ....
(i) 500
(ii) 100
(iii) 1000
(iv) 5000
6. A feedback circuit usually employs .... network.
(i) resistive
(ii) capacitive
(iii) inductive
(iv) none of the above
7. The gain of an amplifier with feedback is known as .... gain.
(i) resonant
(ii) open loop
(iii) closed loop
(iv) none of the above
8. When voltage feedback (negative) is applied to an amplifier, its input impedance ....
(i) is decreased
(ii) is increased
(iii) remains the same
(iv) none of the above
9. When current feedback (negative) is applied to an amplifier, its input impedance ....
(i) is decreased (ii) is increased
(iii) remains the same
(iv) none of the above
10. Negative feedback is employed in ....
(i) oscillators (ii) rectifiers
(iii) amplifiers (iv) none of the above
11. Emitter follower is used for ....
(i) current gain
(ii) impedance matching
(iii) voltage gain (iv) none of the above
12. The voltage gain of an emitter follower is ...
(i) much less than 1
(ii) approximately equal to 1
(iii) greater than 1 (iv) none of the above
13. When current feedback (negative) is applied to an amplifier, its output impedance ......

(i) is increased
(ii) is decreased
(iii) remains the same
(iv) none of the above
14. Emitter follower is a .... circuit.
(i) voltage feedback
(ii) current feedback
(iii) both voltage and current feedback
(iv) none of the above
15. If voltage feedback (negative) is applied to an amplifier, its output impedance ....
(i) remains the same
(ii) is increased (iii) is decreased
(iv) none of the above
16. When negative voltage feedback is applied to an amplifier, its bandwidth ....
(i) is increased (ii) is decreased
(iii) remains the same
(iv) insufficient data
17. An emitter follower has ..... input impedance.
(i) zero (ii) low
(iii) high (iv) none of the above
19. The output impedance of an emitter follower is ....
(i) high (ii) very high
(iii) almost zero (i

20. The approximate voltage gain of an amplifier with negative voltage feedback (feedback fraction being mv) is ....
(i) 1/mv (ii) mv
(iii) 1/1 v + m
(iv) 1 − mv
22. In the expression for voltage gain with negative voltage feedback, the term 1 + Am mv is known as ....
(i) gain factor (ii) feedback factor
(iii) sacrifice factor (iv) none of the above
23
25. Feedback circuit .... frequency.
(i) is independent of
(ii) is strongly dependent on
(iii) is moderately dependent on
(iv) none of the above
26. The basic purpose of applying negative voltage feedback is to ....
(i) increase voltage gain
(ii) reduce distortion
(iii) keep the temperature within limits

(iv) none of the above
27. If the voltage gain of an amplifier without
feedback is 20 and with negative voltage
feedback it is 12, then feedback fraction is
....
(i) 5/3 (ii) 3/5
(iii) 1/5 (iv) 0.033
28. In an emitter follower, we employ ...... negative
current feedback.
(i) 50% (ii) 25%
(iii) 100% (iv) 75%
29. An amplifier has an open loop voltage gain
of 1,00,000. With negative voltage feedback,
the voltage gain is reduced to 100.
What is the sacrifice factor ?
(i) 1000 (ii) 100
(iii) 5000 (iv) none of the above
30. In the above question, what will happen to
circuit performance ?
(i) distortion is increased 1000 times
(ii) input impedance is increased 1000 times
(iii) output impedance is increased 1000
times
(iv) none of the above

1.(ii) 2. (i) 3. (iii) 4. (iv) 5. (ii)
6. (i) 7. (iii) 8. (ii) 9. (i) 10. (iii)
11. (ii) 12. (ii) 13. (i) 14. (ii) 15. (iii)
16. (i) 17. (iii) 19. (iv) 20. (i)
22. (iii) 25. (i)
26. (ii) 27. (iv) 28. (iii) 29. (i) 30. (ii)

Unit 2 Frequency Response of BJT and FET

1) identify the correct relationship
a) f alpha ~ f beta
b) f beta >> f alpha
c) f alpha ~ ft
d) f alpha >> f beta

2) lower cutoff &higher cutoff frequency of rc coupled amplifier are
a) both zero
b) both infinity
c) zero & infinity respectively
d) similar to those of CE stage

3) voltage gain of an amplifier reduces to 1/(root 2)its max
a) break frequency
b) miller frequency

c) half power frequency
d) cutoff frequency

4) rce >> rbe condition is applicable in hybrid -pie equivalent of CE amplifier because
a) collector base junction is reverse biased & emitter base junction is forward biased
b) o/p R is always much larger than i/p R
c) b is the internal base terminal
d) base region is extremely tin compared to emitter & collector terminals

5) expression for short circuit current gain bandwidth
[d]
a) gm/2pie hfe (ce+cc)
b) gm/(ce+cc)
c) gm/ hfe (ce+cc)
d)gm/2pie (ce+cc)

6) identify the expression for voltage gain CE & fet amplifier at low frequency [c]
a) -gm rd Rl /(rd + Rl)
b) gm rd Rl / (rd +Rl+ gm rd Rl)
c) gm rd Rl /(rd + Rl)
d) Rl || rd / (1+ gm rd)

7) Resultant phase shift of even no of CB amplifier stage at frequency below lower cutoff frequency [d]
a) always a multiple of 2 pie
b) product of phase shift introduced by individual stages
c) always 1800
d) sum of the phase shifts introduced by individual stages

8) Identify the incorrect statement for a high frequency hybrid pie model of a BJT is [a]
a) high frequency hybrid pie capacitances can be expressed in terms of low frequency hparameters
b) capacitance between collector & base terminal of a BJT is called overlap -diode capacitance
c) ' B' represent internal base terminal
d) high frequency hybrid pie conductances can be expressed in terms of low frequency hparameters.
9) identify false statement [c]
a) fbeta & Ic exhibits a peak value of a particular ic.
b) unity gain band width Ft is the function of Ic
c)ft & Ic both are functions of f beta
d) Ft variation with Ic is similar to hfe variation with T
ans: [C]

10) during the mid band frequency the gain of amplifier is [d]
a) 1/(root 2) times Max value
b) min
c)unity
d) constant
ans: [D]

11) bandwidth of an amplifier with lower & higher cutoff frequency Fl & Fh .& quantity factor Qis [a]

a) Fh - F l
b) Fh/ q
c) (Fh-Fl)/1.414
d) q-Fl
ans: [A]

12) identify the expression for voltage gain CD & fet amplifier at low frequency
[b]
a) -gm rd Rl /(rd + Rl)
b) gm rd Rl / (rd +Rl+ gm rd Rl)
c) gm rd Rl /(rd + Rl)
d) Rl || rd / (1+ gm rd)
ans: [B]

13) the transconductance gm of a transistor depend on
[b]
a) temperature
b) operation frequency
c) CE voltage
d) C c
ans : [B]

14) ft for a ce amplifier is defined as
[b]
a) the frequency at which the CE current gain falls to half its Max value
b) frequency at which CE current gain becomes unity
c) frequency at which CE voltage gain falls to half its Max value
d) frequency at which CE voltage gain becomes unity
15) the capacitance determining the corner frequency lag network at the i/p of CE amplifier is
[b]
a) miller i/p capacitor
b) c wiring
c) external capacitor at the base
d)cbe
ans: [B]

16) if Av is the voltage gain of an amplifier in db & Ai is its current gain in db then power gain of amplifier in db is [d]
a) Av- Ai
b) Av/ Ai
c)10log 10 Av/ Ai
d) Av+Ai
ans : [D]

17) at frequency below lower cut off frequency in CE amplifier coupling capacitor at the base of the amplifier form an LPF [b]
a) with emitter resistance
b) with i/p resistance
c) with o/p resistance

d) with base resistance
ans: [B]

18) advantage of impedance type inter stage coupling is
[c]
a) very wide band & frequency independent gain curve
b) flat response of frequency in mid band region
c) no dc voltage drop across collector load
d) no requirement of bulky components all frequency
ans: [C]

19) resultant phase shift of odd number of CE amplifier stages at mid band frequency is [b]
a) 3600
b)1800
c) 450
d) 900

20) lower cutoff & higher cut off frequency of an rc coupled amplifier are
[c]
a) both zero
b) both infinity
c) similar to of CE stage
d) zero& infinity
ans: [C]
21) higher cutoff frequency of transistor amplifier is mainly because of
[a]
a) inter electrode capacitance
b) bypass capacitance
c) blocking capacitance
d) coupling capacitance

22) ratio of slopes of the gain curve of an amplifier below lower cutoff frequency & above cutoff frequency is [b]
a) 3
b) unity
c)2
d) 6
ans: [B]

23) the capacitors that are short circuited at low frequencies in CE amplifier are
[d]
a) o/p coupling capacitors
b) i/p coupling capacitors
c) emitter bypass capacitors
d) inter electrode capacitor
ans:[B]

24) the critical capacitance that determines the overall cut off frequency of an amplifier is the one which sees an equivalent resistance [a]

a) of minimum value
b) of Max value
c) of infinity value
d) equals to its reactance value at that frequency
ans: [A]

25) distortion in amplifiers due to unequal amplitude gains at different frequencies is referred to as [c]
a) phase shift distortion
b) amplitude distortion
c) frequency distortion
d) delay distortion
ans : [C]

26) slope of the gain curve of an amplifier below cut off frequency is
[a]
a) -20 db decade
b) 6 db decade
c)-6 db decade
d) 20 db decade
ans : [A]
28) the CE short circuit current gain in db at frequency f = Ft is
[d]
a) hfe/1.414
b) unity
c) hfe
d)zero
ans: [D]

29). Phase difference between o/p and i/p voltages of a transistor amplifier at lower cut off frequencies is
a)180 b) 45 c) 0 d) 90
Ans: (b)

30) All frequencies below lower cut off frequency in a CE amplifier, the coupling capacitor at the base of the amplifier forms a LPF
a)with RE b)Rip c)RB d)Rop
Ans: (b)

Unit 3

Multivibrators Non Linear Wave Shaping

1. A circuit which can oscillate at a number of frequencies is called a __.
2. Basically there are __ types of multivibrators. They are __, __ and __.
3. Resistive coupling is called __ coupling and capacitive coupling is called ___ coupling.
4. A __ multivibrator is the basic memory element.
5. In bistable multivibrators, the coupling elements are __.
6. In monostable multivibrator, the coupling elements are __.
7. In astable multivibrator, the coupling elements are __.

8. A __ circuit is one which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other.
9. A bistable multivibrator is also called __ , __, __, ___ and __.
10. A __ multivibrator is used to perform many digital operations such a counting and storing of binary information. It is also used in the generation and processing of pulse type waveform.
11. A __ of a binary is one in which the currents and voltages satisfy Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of loop gain being less than unity is satisfied.
12. A __ state of a binary is one in which the device can remain permanently.
13. Loop gain will be __ if either of the two devices is below cut-off or if either device is in saturation.
14. In the stable state, the loop gain is __
15. During transition, the loop gain is __
16. The change in collector voltage resulting from a transition from one state to the other is called __ and is given by ___.
17. __ reduces the output swing.
18. The flip-flop circuit components must be chosen so that under the maximum load which the binary drives, one transistor remains in ___ while the other is __.
19. A constant output swing and a constant base saturation current can be obtained by clamping the collectors to an auxiliary voltage V __ Vcc through the diodes D1 and D2.
20. The diodes used in a bistable multivibrator to maintain a constant output swing are called __ diodes.
21. The interval during which conduction transfers from one transistor to another is called the __.
22. The transition time may be reduced by shunting the coupling resistor with __ called the __
23. Commutating capacitors, also called __ or __ capacitors are used to increase the speed of operation.
24. The smaller allowable interval between triggers is called the __ of the flip-flop.
25. The reciprocal of the resolving time of the flip-flop is the __ at which the binary will respond.
26. The additional time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the __.
27. The sum of the transition time and the settling time is called the __.
28. If the commutating capacitors are too small, the __ time is increased and if they are too large the ___ time increased.
29. The resolution time of a binary can be improved by a) __ , b) __ and c) ___.
30. The disadvantages of non-saturated binary are a) ___, b) ___ and c) ___.
31. The application of an external signal to induce a transition from one state to the other is called __.

1. __ is the process of cutting and removing a part of the waveform.
2. __ circuits are used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference voltage level.
3. Clipping circuits are also called __ or __ limiters, __ selectors or ___.
4. Clipping circuits do not require __ elements.
5. In the simple clipping circuits, the external resistance R is selected to be the __ of the diode forward and reverse resistance, i.e. R = __
6. The use of the diode as a series element has the disadvantage that __
7. The use of the diode as a shunt element has the disadvantage that __
8. A transistor has __ nonlinearity which can be used for clipping purpose.
9. A diode has __ nonlinearity which can be used for clipping purposes.
10. Single ended clipping is also called __ clipping.
11. Double ended clipping is also called __ clipping.
12. In a diode, the nonlinearity occurs when it goes from _- to ___

13. In a transistor, the nonlinearities occur when a) the device goes from __ region to __ region and b) the device goes from __ region to __ region.
14. the emitter coupled clipper is a __ clipper. It is an emitter coupled __ amplifier.
15. A clipping circuit may be used to convert a sine wave into a __ wave.
16. A __ circuit is one, which may be used to mark the instant when an arbitrary waveform attains some particular reference level.
17. Comparators may be __ comparators or __ comparators.
18. __circuits may be used as comparators
19. Clipping circuits are __ comparators.
20. The Schmitt trigger is a __ comparator.
21. Regenerative comparators employ __feedback.
22. In a __ clipper, when the diode is OFF, the output follows the input.
23. In a ___ clipper, when the diode in ON, the output follows the input.
24. Clipping circuits differ from comparators in that __.
25. An example of a non-regenerative comparator is a __.
26. An example of a regenerative comparator is a __
27. The Schmitt trigger comparator generator generates approximately __
28. The blocking oscillator comparator generates ___
29. ___ are used to fix the positive or negative extremity of a periodic waveform at some constant reference level.
30. Under steady-state condition, the clamping circuits restrain the __ of a waveform going beyond VR.

UNIT4 Large Signal Amplifiers and Linear Wave Shaping

1) Non-linear distortion is maximum in
a) class
B mode
b) class A mode
c) class AB mode
d) class C mode

2) final stage of multistage amplifier is generally a) a
pre-amplifier
b) a voltage post amplifier
c) a power amplifier
d) a microphone amplifier
3) Max conversion efficiency of a series fed class A power amplifier is
a) 75
b) 100
c) 50
d) 25
4) even harmonics are not present in the o/p of
a) class A transformer coupled amplifier
b) class c amplifier
c)class A amplifier
d) class B push pull amplifier

5) Even harmonics in the o/p are connected in push - pull configurations only if

[a]
a) both transistors are perfectly matched
b) both NPN & PNP transistors are used
c) A phase inversion is not used at inputs of 2 transistors
d) two power supplies are used
ans:[A]

6) i/p signals swing in class A power amplifier is restricted to
[d]
a) a small portion around Q point in active region
b) entire portion around Q point in saturation
c) entire portion around Q point in cutoff
d) entire portion around Q point in active
ans: [D]
7) transistor in class C amplifier is based beyond cutoff region to
[b]
a) ensure reduced distortion of o/p signal
b) ensure conduction angle of less than 1800
c) ensure conduction angle of transistor for entire i/p cycle
d) ensure o/p wave shape to the replica of i/p wave shape
ans: [B]

8) increased conversion efficiency in class B over class A operation is mainly due to
[b]
a) elimination of all higher harmonics
b) elimination of dc current in the load
c) usage of single power supply
d) elimination of cross over distortion
ans: [B]

9). The frequency at which CE is short circuit current gain becomes unity is represented by__fT_______
71. Non linear distortion is maximum in
a) Class B mode a) Class A mode
a) Class AB mode d) a) Class C mode
Ans: (b)

10). Even harmonics are not present in the o/p of Class B push pull amplifier.

11) Cross over distortion in class B amplifier is due to
(a) finite cut-off voltage of the two transistors
(b) non-identical behaviour of the two transistors
(c) elimination of two power supplies in the circuit
(d) elimination of even harmonics in the o/p
impedance

1. A Network which can be mathematically described by linear constant coefficient different equations is called a __.
2. The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called __.

3. Except for the __ signal, no other signal can preserve its form when it is transmitted thorough a linear network.
4. A __ circuit passes low frequency signals and attenuates high frequency signals.
5. The frequency at which the gain is __ of its maximum value is called the cut-off frequency.
6. The lower cut-off frequency of a low pass circuit is __.
7. The upper cut-off frequency of a high pass circuit is __ and is equal to its __ and is given by f_2 = __.
8. At very high frequencies, the capacitor acts almost as a __ and at very low frequencies, the capacitors acts almost as an __.
9. The capacitor __ the dc signal.
10. At the cut-off frequency of the RC circuit, the ___ reactance is equal to the __ and the gain is ___.
11. A signal which maintains the value zero for all times $t < 0$, and maintains the value V for all times $t \geq 0$, is called a __.
12. The expression for the output of a low pass circuit excited by a step input is v_0 = ___.
13. __ is defined as the time taken by the output to rise from 10% to 90% of its final steady-state value for a step input.
14. The rise time of a waveform is directly proportional to the __ and inversely proportional to the __.
15. The rise time t_r of a waveform is given by t_r = ____.
16. In an RC circuit, for a step input, if the initial slope of the output voltage across the capacitor is maintained constant, the output reaches its final value in one ___.
17. For the most applications, the steady-state condition is assumed to be reached at t =____.
18. A pulse may be treated as the sum of a __ followed by a delayed __ of the same amplitude.
19. A pulse shape is preserved when it is passed through a low-pass circuit, if the 3-dB frequency is approximately equal to the __ of the pulse width.
20. A periodic waveform which maintains itself at one constant level V' with respect to ground for a time T_1, and then changes abruptly to another level V" and remains constant at that level for a time T_2, and repeats itself with a period $T=T_1+T_2$ is called a __.
21. Under ___ conditions, the capacitor in the RC circuits charges and discharges to the same level in each cycle. So the shape of the output waveform is fixed.
22. A waveform which is zero for $t < 0$ and which increases linearly with time for $t > 0$ is called a ___ or ___.
23. At the end of a ramp input, the difference between the input and the output divided by the input is called the ___.
24. If two stages whose individual rise times are t_{r1} and t_{r2} respectively are cascaded, the rise time of the output waveform will be t_r = ____.
25. A low pass circuit acts as __ if the time constant of the circuit is very large in comparison with the time required for the input signal to make an appreciable change.
26. For an RC low-pass circuit to act as an integrator, it is necessary that RC ___ where T is the period of the sine wave.
27. A __ attenuates all low frequency signals and transmits only signals of high frequency.
28. The lower cut-off frequency of a high pass circuit is ___ and is given by f1 = __.
29. The upper cut-off frequency of a high pass circuit is ___ and hence its bandwidth = ___.
30. The capacitor in the high-pass circuit blocks the dc component of the input from going to the output. Hence it is called a __.

Unit 5 **Switching characteristics of Devices**

1. The static resistance of a diode is the ratio of _- to __

2. the dynamic resistance of a diode is the ratio of __ to __
3. When a diode is reverse biased, it acts as an __ switch, and when it is forward biased, it acts as a __ switch.
4. In the steady state condition, the current which flows, through the diode is a __ current.
5. The __ current results from the gradient of the minority carriers.
6. At large current amplitudes, the diode behaves as a combination of a __ and __.
7. At intermediate currents, the diode behaves as a __ , ___ and a __.
8. At low currents, the diode is represented by a parallel combination of a __ and __.
9. The forward recovery time t_{fr} is the time difference between the __ and the time when this voltage reaches and remains within __.
10. The __ recovery time of a diode does not usually constitute a problem.
11. The time required for the stored minority charge to become zero after the application of the reverse voltage is called the __.
12. The time which elapses between the instant when the stored minority charge becomes zero and the time when the diode has nominally recovered is called the __.
13. A large signal approximation which often leads to a sufficient accurate engineering solution is the __ representation.
14. Once breakdown occurs, the diode current can be controller only by the resistance of the ___.
15. The breakdown due to thermally generated carriers is called the __ breakdown.
16. The breakdown due to existence of strong electric fields is called the __ breakdown.
17. __ breakdown occurs at voltages below 6 V.
18. The operating voltages in __ breakdown are from several volts to several hundred volts.
19. The breakdown voltage of a Zener diode __with temperature where as the breakdown voltage of an avalanche diode __ with temperature.
20. The breakdown voltage for a particular diode depends on the __ levels in the junction.
21. When a transistor is in saturation, junction voltages are __ but the operating currents are __.
22. When a transistor is in cut off, the junction voltages are ___ but the currents are __.
23. For Ge, Vv = ____ . For Si, Vv = _____. For avalanche diodes, Vv=___.
24. The time required for the current to rise to 10% of its saturation value after the application of the input is called the ___.
25. The time required for the current to rise from 10% to 90% of the saturation value is called the __.
26. The sum of the delay time and the rise time of a transistor is called the __ time.
27. The interval which elapses between the transition of the input waveform and the time when Ic has dropped to 90% of saturation current is called the __.
28. The time required for Ic to fall from 90% to 10% of its saturation level is called the __.
29. The sum of the storage time and the fall time of a transistor is called the __ time.
30. A transistor can operate in three regions : ___, ____ and ___.

20. Tutorial Problems

Tutorial class-1

- Classification of amplifiers& distortion in amplifiers.
- Analysis of CE, CB configurations with Hybrid model.
- Design of single stage amplifier using BJT.
- Miller’s theorem its dual.
- The concept of feedback & advantages and disadvantages
- Classification of feedback amplifiers.

- Characteristics of negative feedback & its effect on amplifiers.
- Voltage series &shunt, current series& shunt feedback configurations.

Tutorial Class-2

- Frequency response of single stage BJT amplifier.
- Effect of coupling &bypass capacitors on frequency response.
- The hybrid model at high frequencies.
- Gain bandwidth product.
- Small signal model of a MOS transistor.
- CS amplifier with resistive load using small signal model.
- CS amplifier with diode connected load using small signal model.
- CG cascode and folded cascode amplifier and its analysis using small signal model?

Tutorial Class-3

- Design a monostable multivibrator circuit that produces a pulse width of 10ms. Assume hfe= 30, $V_{CE(sat)}$=0.3V, $V_{BE(sat)}$= 0.7V, $I_{c(sat)}$=5mA, V_{cc}=6V, V_{BB}= -1.5V.
- Silicon transistors with $h_{fe(min)}$ = 30 are available. If V_{cc}= 12V and V_{BB}= 6V, design a fixed bias bistable multivibrator.
- Consider the Schmitt trigger With germanium transistor having hfe= 20. The circuit parameters are V_{CC}=15V, R_S= 2KΩ, R_{C1} = 1KΩ, R_{C2} = 1KΩ, R_1= 3KΩ, R_2= 10KΩ and R_e= 6KΩ. Calculate LTP and UTP.
- If a astable multivibrator has C_1=C_2=1000pF and R_1=R_2=KΩ. Calculate the frequency of oscillation.
- Design a self-biased bistable multivibrator using silicon transistor given V_{CC}=6 V and $h_{fe(min)}$ =30. Assume appropriate junction voltages for your design.
- Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500Hz.
- The input to the diode differentiator comparator is ramp whose slope is 0.1V per second. Reference level is VR=0V. Amplifier gain 10 and τ_1 = τ_2 =100 micro second. What is peak to peak value of output.
- Designa diode clamper to resistor a d.c. level of +3 volts to an input signal of peak value of 10volts. Assume drop across diode is 0.6 volts.
- Draw the transfer characteristics of series clippers.

- Draw the transfer characteristics of shunt clippers.

Tutorial Class-4

- Classification of power amplifiers.
- Class A,B&AB power amplifiers.
- Efficiency of power amplifiers.
- Thermal runaway &heat sinks.
- A step input of 10V when applied to the Low Pass RC circuit produces the output with a Rise time of 200 micro sec. Calculate the upper 3dB frequency of the circuit if the circuit uses a capacitor of 0.47 micro F, Determine the value of the resistance.
- Derive expression for % tilt .
- A step generator of 50ohms impedance applies a 10V step of 2.2 nsec rise time to a series combination of a capacitor C and a resistor R=50ohm. A pulse of amplitude 1V appears across R. Find the value of the capacitance C.
- A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero is applied to RC integrating circuit. The time constant is half the period of the square wave. Find the peak-to-peak value of output voltage.
- 5.What is the ratio of the rise time of the three sections in cascade to the rise time of single section of low pass circuit.

Tutorial Class-5

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- Draw and explain transistor switching times.
- Draw and explain diode switching tines.
- Derive the expression for collector to emitter voltage with open circuit base.
- Derive the expression for collector to emitter voltage with base is short circuited to emitter.
- Derive the expression for collector to emitter voltage with RB in base in series with V_{BB}.

21. Known gaps

Known gaps:

As per the industry levels the following are the known gaps of the EDC subject

Which is in the JNTU curriculum.

1.The subject is not matching with Tuning amplifiers, Multistage amplifiers.
2. Characteristics of MOS transistor to obtain small signal equivalent model
3. Concept of positive feedback its characteristics
4. Tuned circuits its working principle used in tuned amplifiers
5.This subject is not matching with MOS amplifiers.
6. This Subject Is Not Matching Logic Gates Using Diodes & Transistors
7. This Subject Is Not Matching Synchronization And Frequency Division
8. . Applications of Multivibrators
9. Realization of logic gates using CMOS circuits
10. Introduction to counting and timing circuits

Action taken:

Following topics are taken to fill the known gaps

1.cascading and cascade amplifiers.
2.FET amplifiers with different Loads.
3.About tuning amplifiers and realization logic gates using diodes and transistors.

22. Group discussion topics.

1. What is an amplifier?
2. What is small signal amplifier?
3. Explain the usefulness of the decibel unit?
4. Define the term bandwidth of an amplifier?
5. State various capacitances in the hybrid model?
6. Define the term bandwidth of an amplifier
7. Why it is not possible to use the h- parameters at high frequencies?
8. What do you mean by the half power or 3 db frequencies?
9. What are the advantages and disadvantages of negative feedback?
10. Differentiate between voltage and current feedback in amplifiers?
11. What are the types of class B amplifier?
12. Draw a quasi complimentary symmetry power amplifier?
13. What is the advantage of using the output transformer for a class A amplifier?

14. What is the disadvantage of transformer coupled class A amplifier
15. What happens when a sine wave is applied to a differentiator or integrator circuit?
16. What is the ideal value of phase shift offered by an RC circuit?
17. Show theoretically how you get a triangular wave when a square wave is given to a integrator?
18. What happens when a sine wave is applied to a differentiator or integrator circuit?

23.References, Journals, websites and E-links

REFERENCES

1.Introductory Electronic Devices and Circuits(conventional flow version)-Robert T.Paynter,7th edition,2009,PEI.

2. Electronic Devices and Circuits – Anil K. Maini, Varsha Agarwal, 1 Ed., 2009, Wiley

3. Pulse, Digital and Switching Waveforms - J. Millman, H. Taub and Mothiki S Prakash rao,2nd edition,TMH.

WEBSITES

1. www.basicelectronic.blogspot.com
2. www.modernelectronics.org
3. www.electronicsforyou.con
4. **www.npteliitm.ac.in**

JOURNALS

1. A Very Low Level DC Current Amplifier Using Photocoupler Negative Feedback Circuit .

2. On the class IF power amplifier design

3. A Ringing Surge Clamper Type Active Auxiliary Edge-Resonant DC Link Snubber-Assisted Three-Phase

24.Quality Control Sheets

a) Course end survey

b) Teaching Evaluation

C)hard copy will attach at the end of the course of course end survey and Teaching Evalution

Closure Report:

1. Total Number of classes planned - 60
2. Total Number of classes actually taken - 75
3. Total Number of students attended for the internal exam -
4. Total Number of students attended for the external exam -
5. Total number of students passed the exam -
6. Pass percentage -